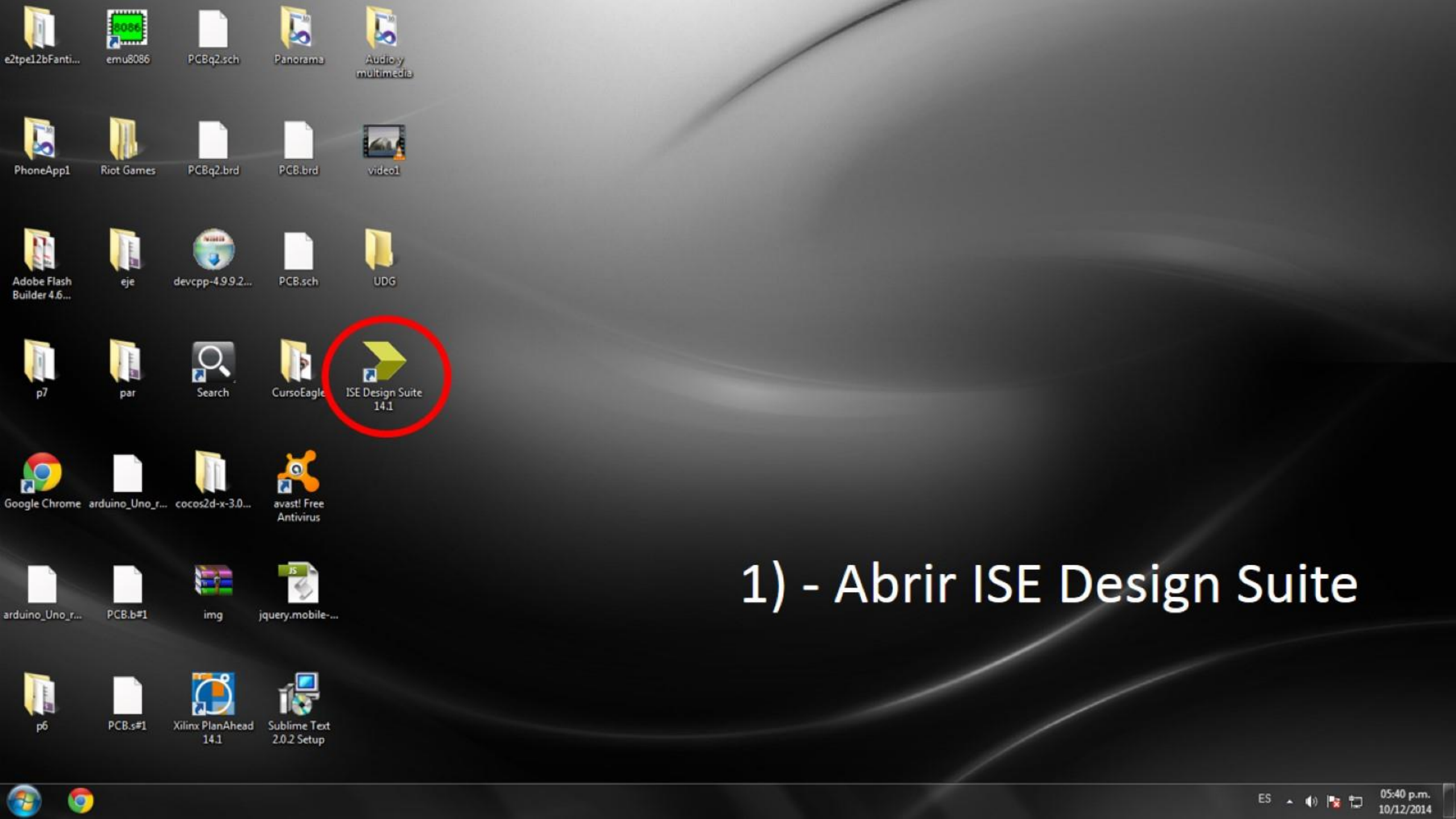
Spartan 6

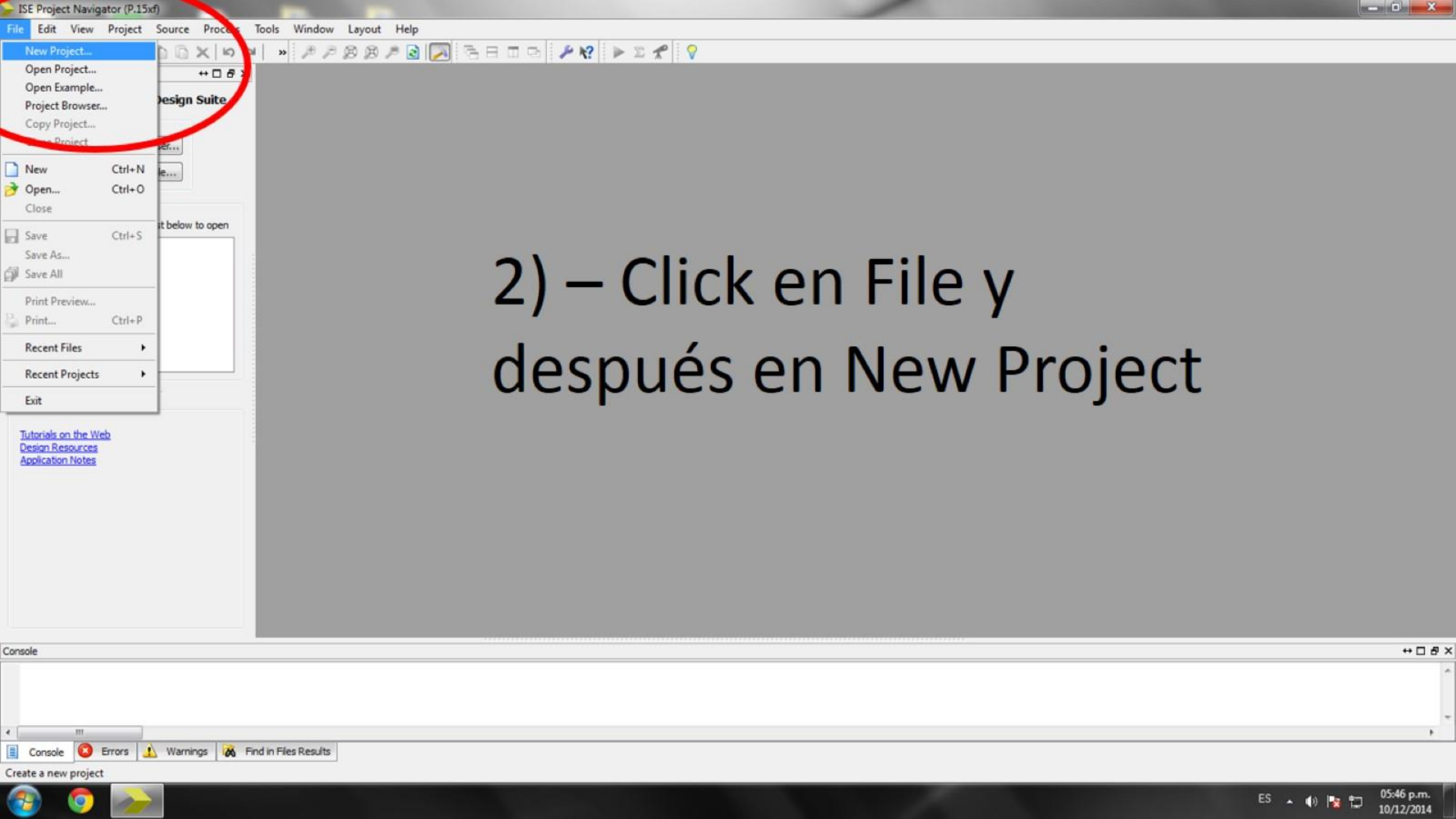
Laboratorio de programación de sistemas en tiempo real

Prestadores de servicio:
Jonathan Muñoz Santiago
Rogelio Rosales de la Mora

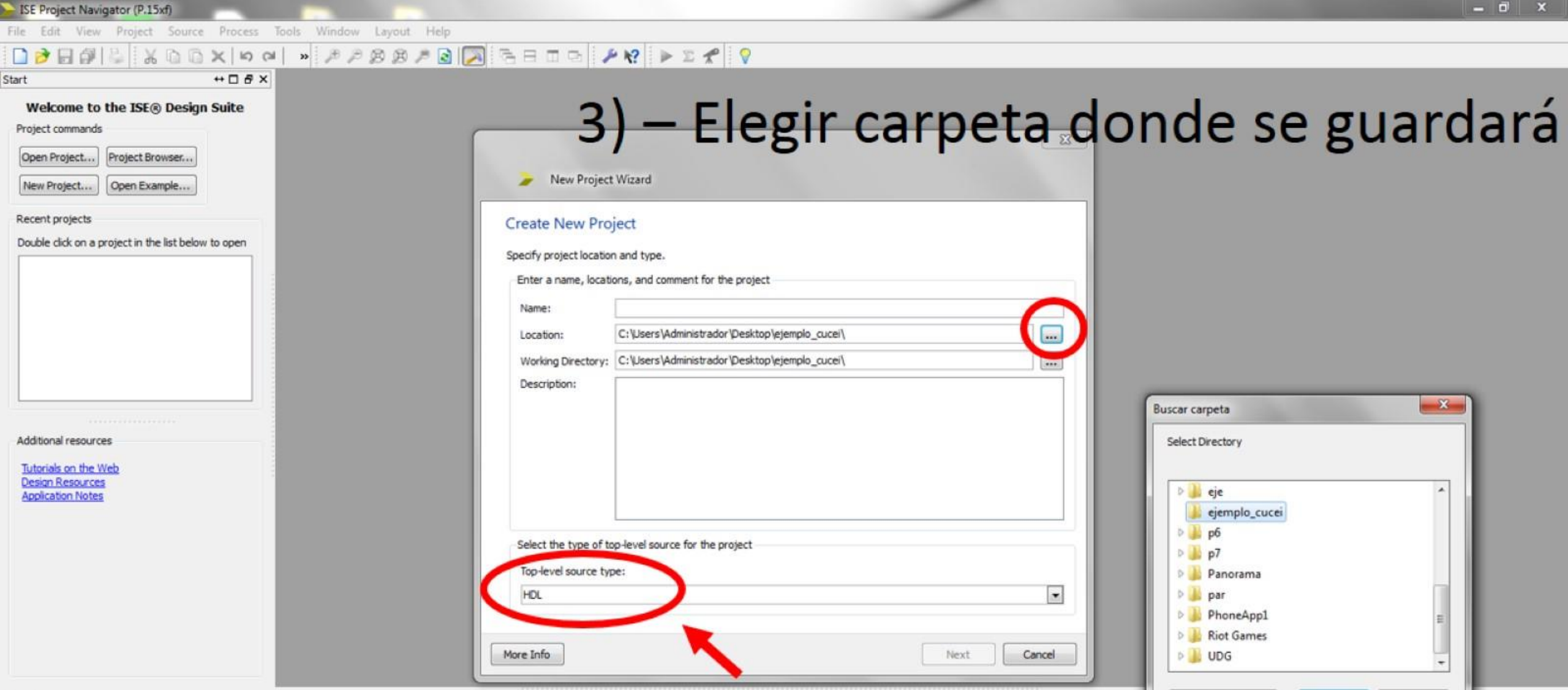
Jefe del laboratorio de sistemas:
Profesor José Juan Meza Espinoza

Profesor de apoyo y soporte
Profesor Salomon Eduardo Ibarra Chavez

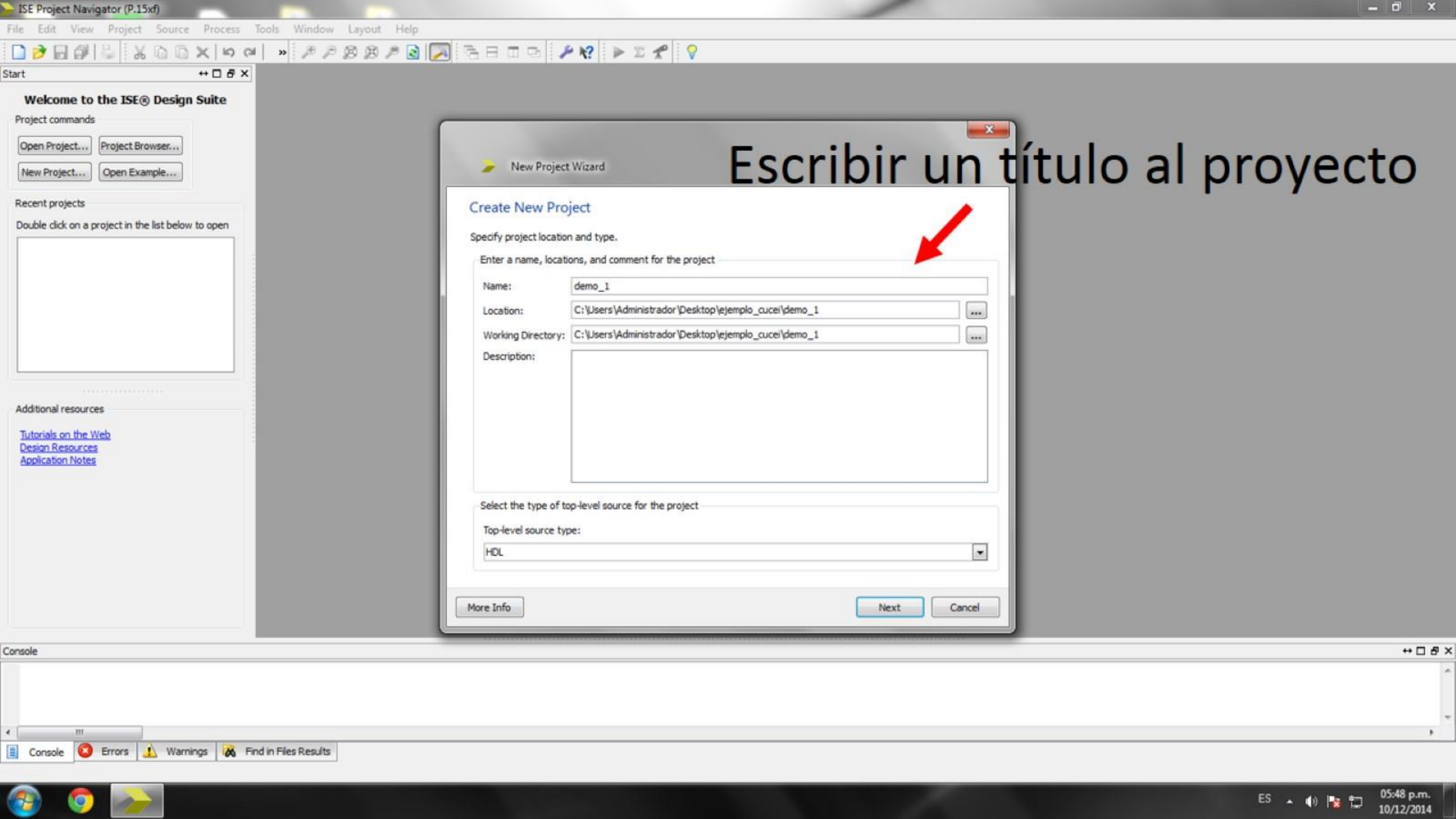

e2tpe12bFanti...
emu8086
PCBq2.sch
Panorama
Audio y multimedia
PhoneApp1
Riot Games
PCBq2.brd
PCB.brd
video1
Adobe Flash Builder 4.6...
eje
devcpp-4.9.9.2...
PCB.sch
UDG
p7
par
Search
CursoEagle
ISE Design Suite 14.1
Google Chrome
arduino_Uno_r...
cocos2d-x-3.0...
avast! Free Antivirus
arduino_Uno_r...
PCB.b#1
img
jquery.mobile-...
p6
PCB.s#1
Xilinx PlanAhead 14.1
Sublime Text 2.0.2 Setup
1) - Abrir ISE Design Suite
ES
05:40 p.m.
10/12/2014

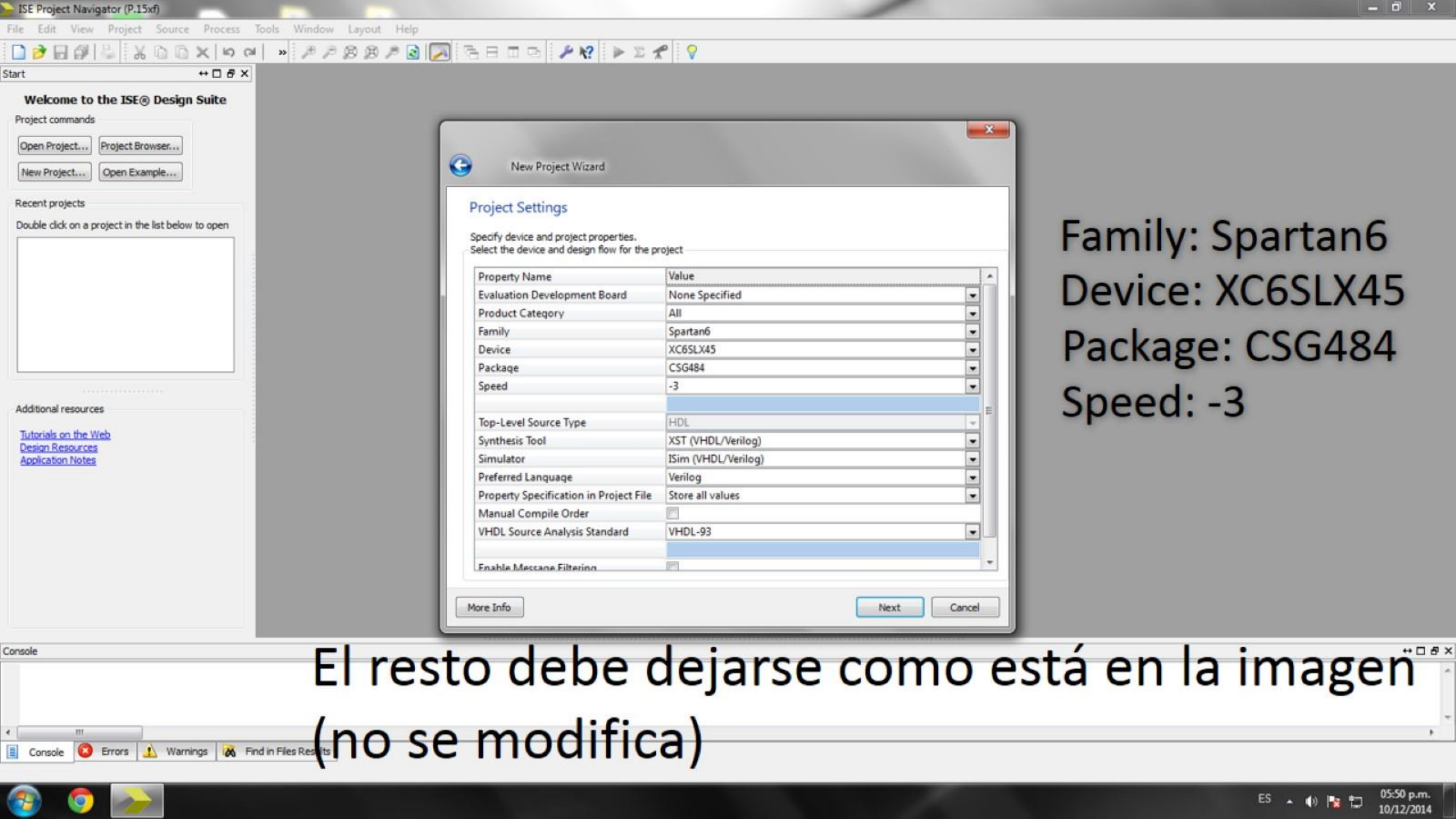

ISE Project Navigator (P.15xf)
File
Edit
View
Project
Source
Tools
Window
Layout
Help
New Project...
Open Project...
Open Example...
Project Browser...
Copy Project...
New Ctrl+N
Open... Ctrl+O
Close
Save Ctrl+S
Save As...
Save All
Print Preview...
Print... Ctrl+P
Recent Files
Recent Projects
Exit
Tutorials on the Web
Design Resources
Application Notes
2) – Click en File y
después en New Project
Console
Console
Errors
Warnings
Find in Files Results
Create a new project
ES
05:46 p.m.
10/12/2014

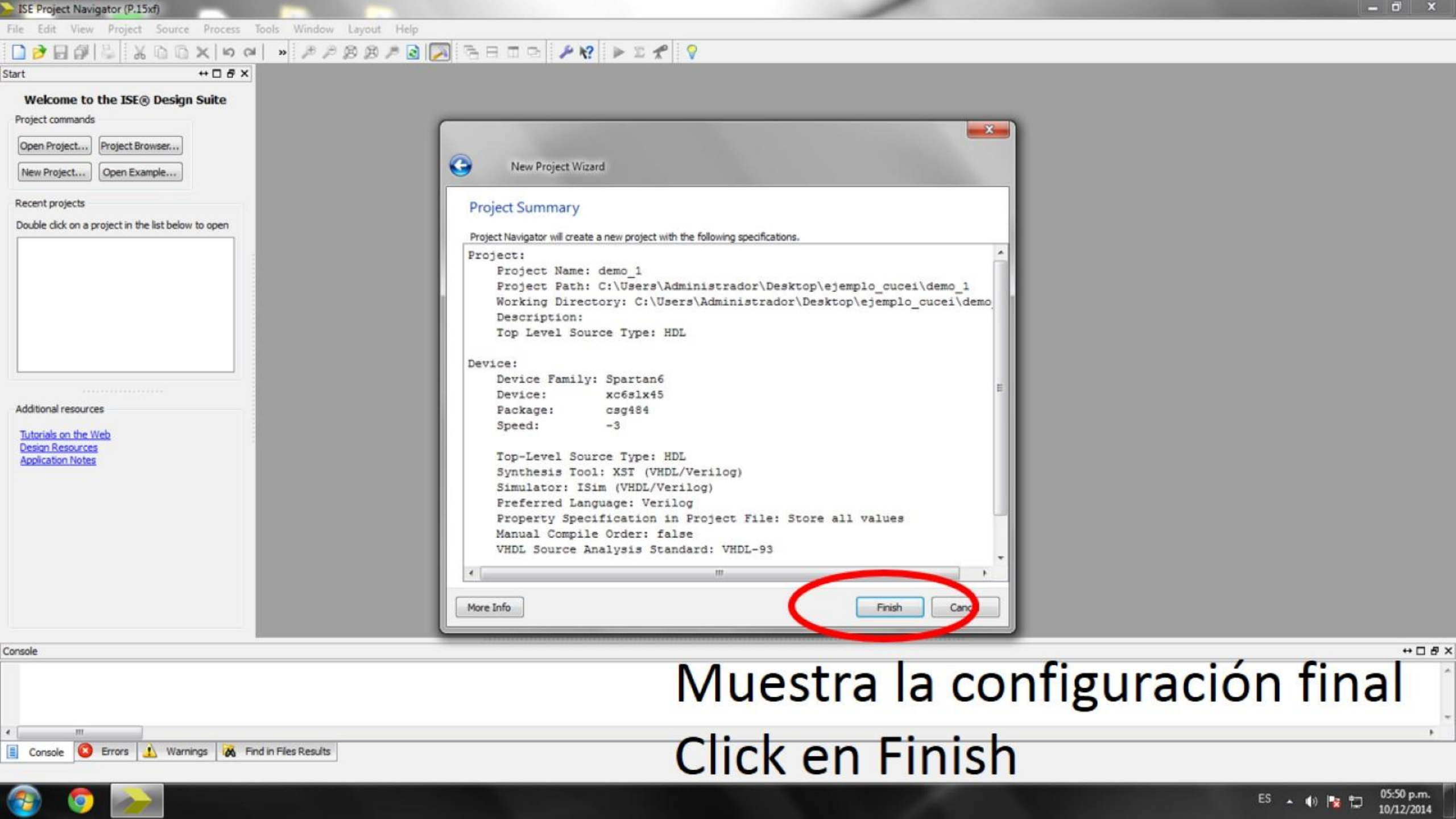
3) – Elegir carpeta donde se guardará

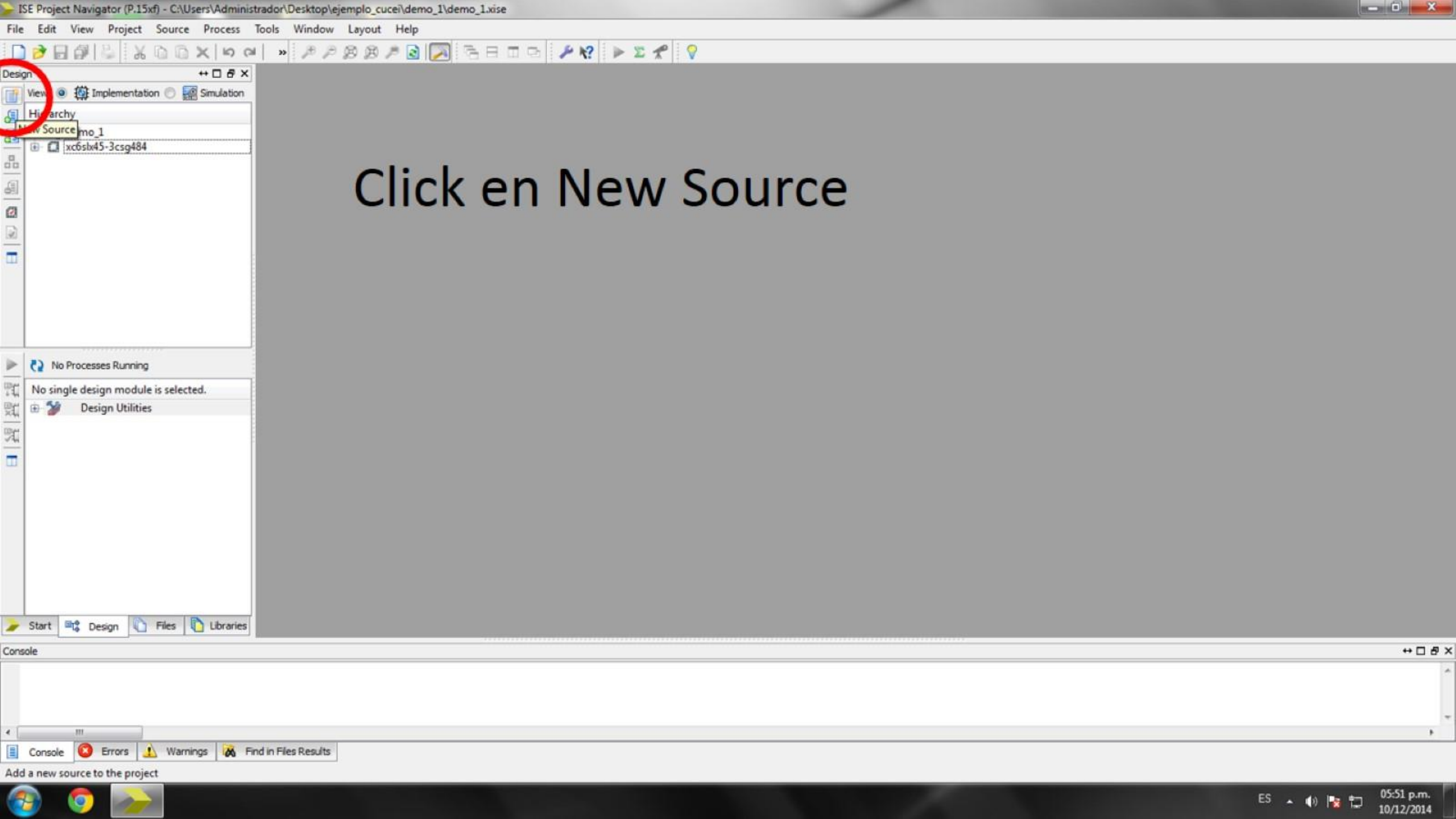


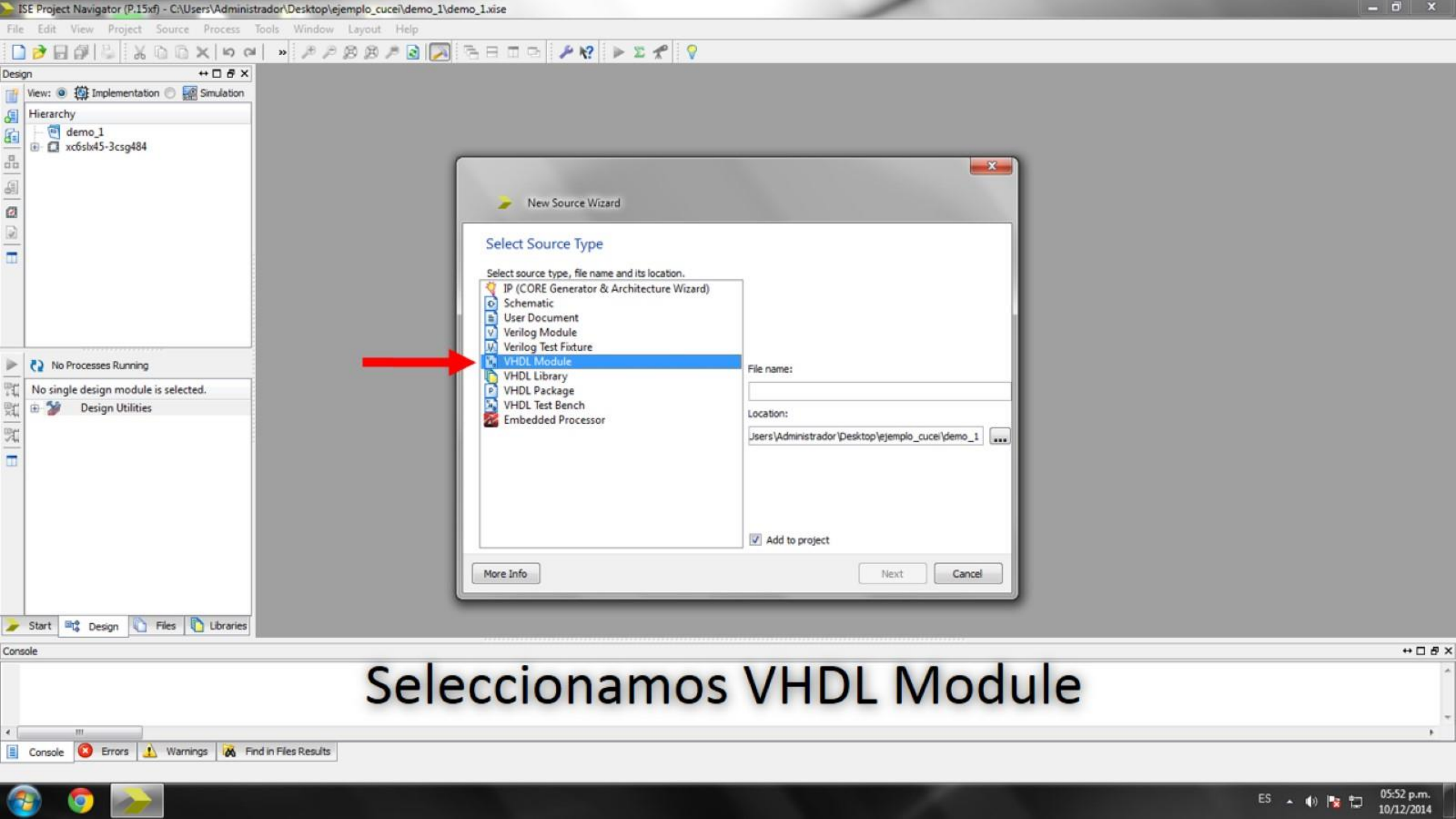
*Debe estar en HDL


ISE Project Navigator (P.15xf)
File Edit View Project Source Process Tools Window Layout Help
Start
Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Double click on a project in the list below to open
Additional resources
Tutorials on the Web
Design Resources
Application Notes
Escribir un título al proyecto
New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name: demo_1
Location: C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1
Working Directory: C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1
Description:
Select the type of top-level source for the project
Top-level source type:
HDL
More Info
Next
Cancel
Console
Console
Errors
Warnings
Find in Files Results
ES
05:48 p.m.
10/12/2014

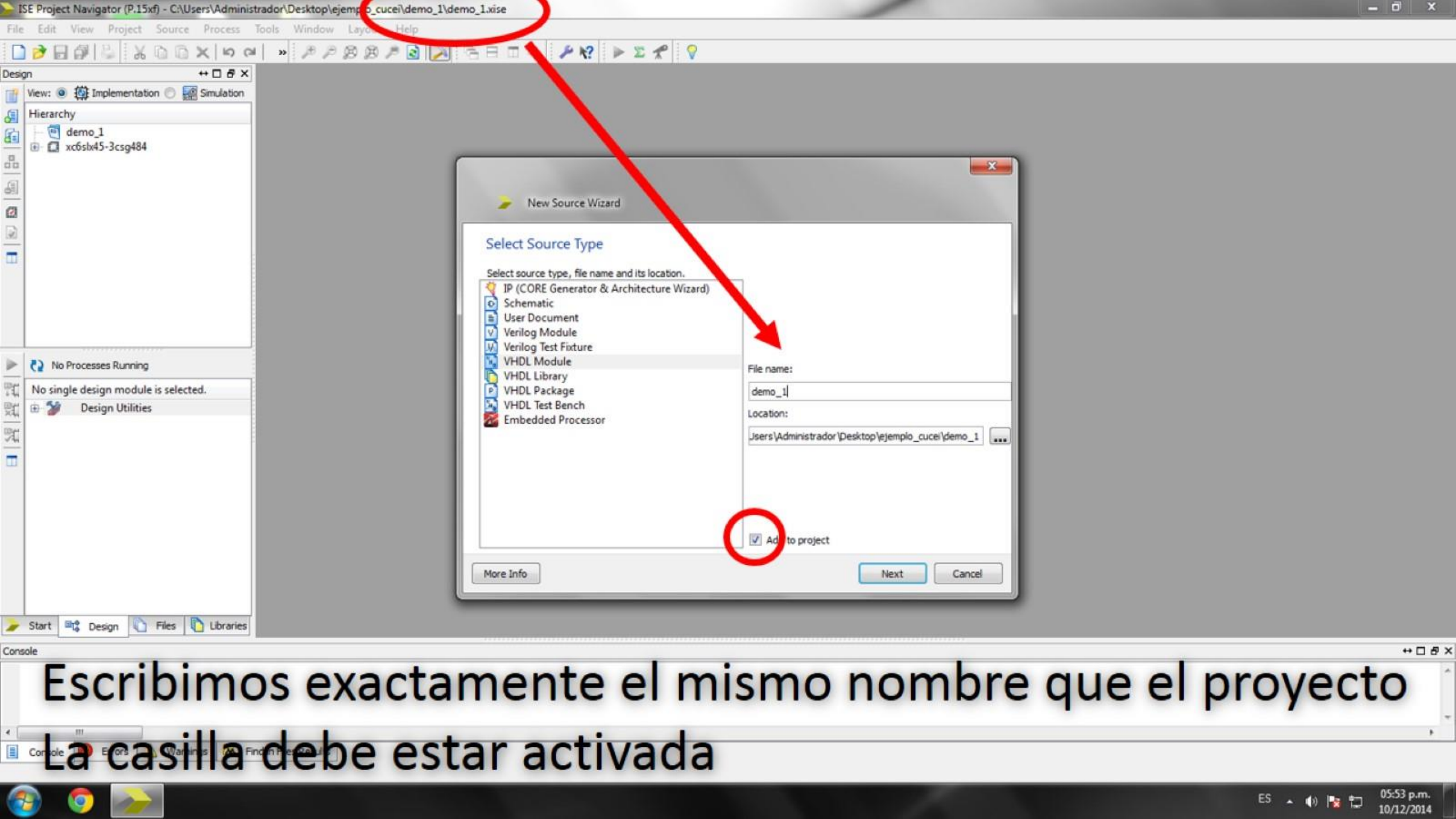

ISE Project Navigator (P.15xf)
File Edit View Project Source Process Tools Window Layout Help
Start
Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Double click on a project in the list below to open
Additional resources
Tutorials on the Web
Design Resources
Application Notes
New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Spartan6
Device
XC6SLX45
Package
CSG484
Speed
-3
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
More Info
Next
Cancel
Family: Spartan6
Device: XC6SLX45
Package: CSG484
Speed: -3
Console
Errors
Warnings
El resto debe dejarse como está en la imagen
(no se modifica)
ES
05:50 p.m.
10/12/2014

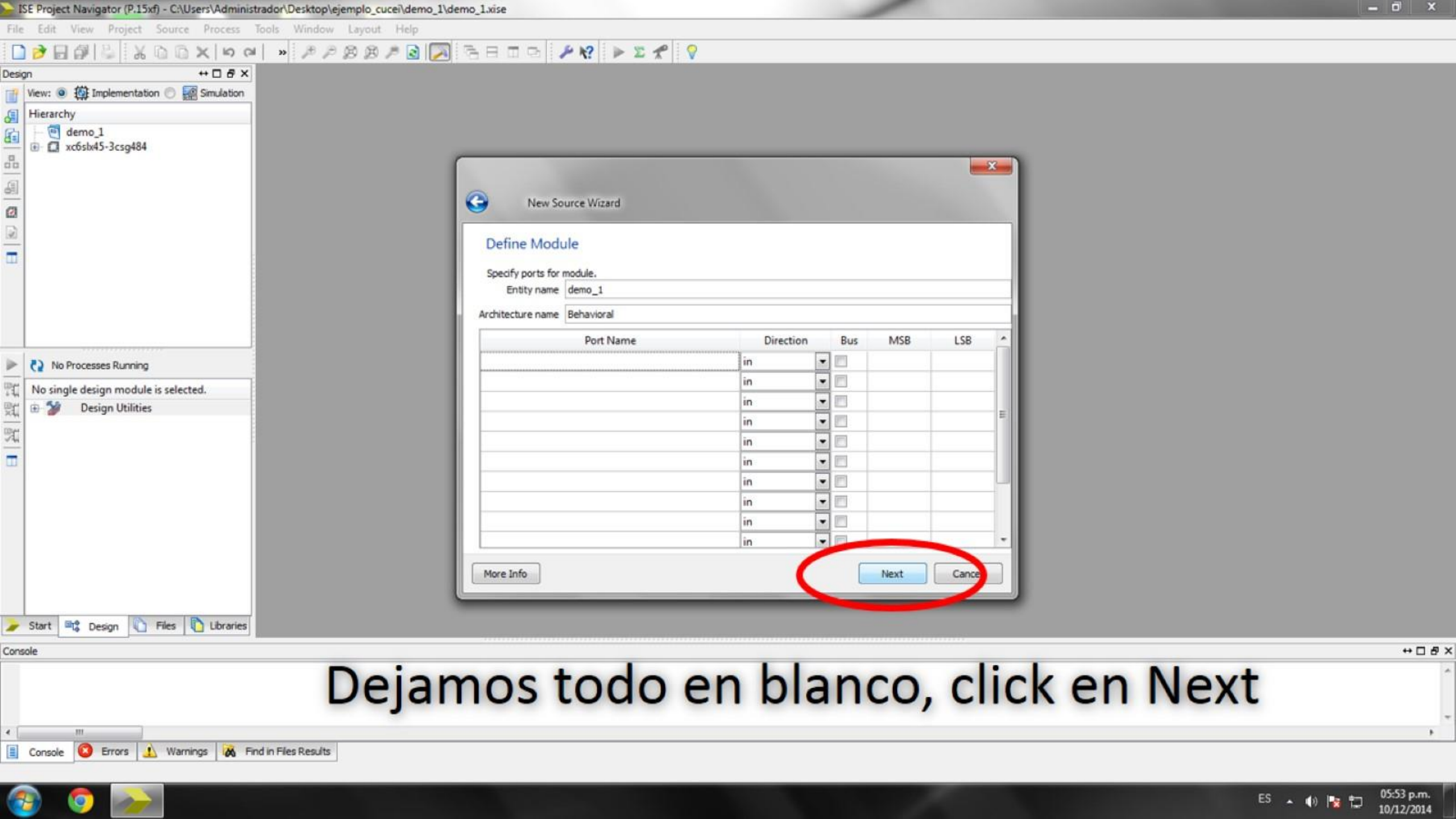

ISE Project Navigator (P.15xf)
File Edit View Project Source Process Tools Window Layout Help
Start
Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Double click on a project in the list below to open
Additional resources
Tutorials on the Web
Design Resources
Application Notes
New Project Wizard
Project Summary
Project Navigator will create a new project with the following specifications.
Project:
Project Name: demo_1
Project Path: C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1
Working Directory: C:\Users\Administrador\Desktop\ejemplo_cucei\demo
Description:
Top Level Source Type: HDL
Device:
Device Family: Spartan6
Device: xc6slx45
Package: csg484
Speed: -3
Top-Level Source Type: HDL
Synthesis Tool: XST (VHDL/Verilog)
Simulator: ISim (VHDL/Verilog)
Preferred Language: Verilog
Property Specification in Project File: Store all values
Manual Compile Order: false
VHDL Source Analysis Standard: VHDL-93
More Info
Finish
Canc
Console
Console
Errors
Warnings
Find in Files Results
Muestra la configuración final
Click en Finish
ES
05:50 p.m.
10/12/2014

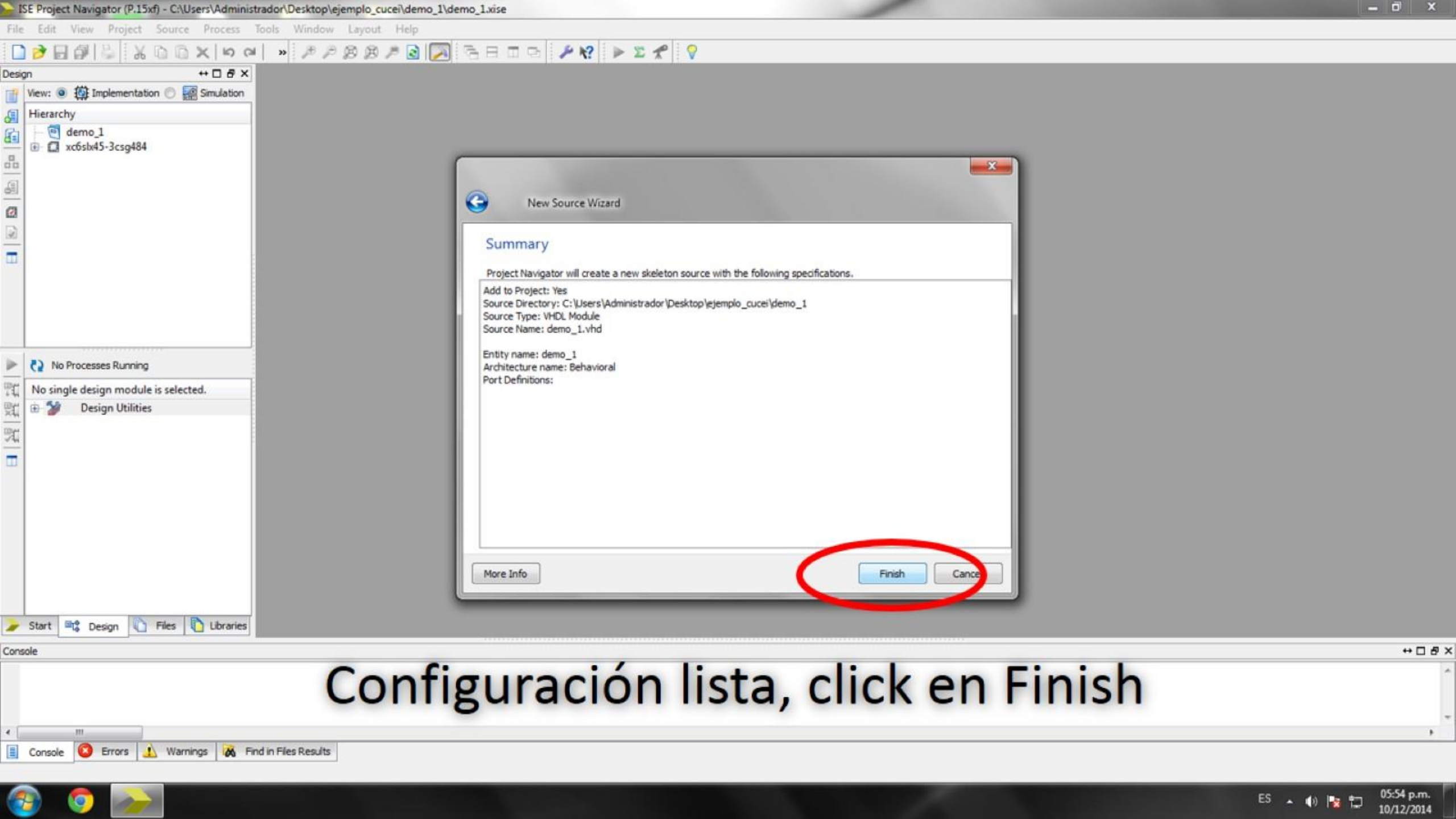

ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
New Source
xc6slx45-3csg484
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
Click en New Source
Console
Console Errors Warnings Find in Files Results
Add a new source to the project
ES
05:51 p.m.
10/12/2014



Seleccionamos VHDL Module


ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
demo_1
Location:
Users\Administrador\Desktop\ejemplo_cucei\demo_1
Add to project
More Info
Next
Cancel
Console
Escribimos exactamente el mismo nombre que el proyecto
La casilla debe estar activada
ES
05:53 p.m.
10/12/2014


ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
New Source Wizard
Define Module
Specify ports for module.
Entity name demo_1
Architecture name Behavioral
Port Name Direction Bus MSB LSB
in
More Info
Next
Cancel
Console
Errors Warnings Find in Files Results
Dejamos todo en blanco, click en Next
ES
05:53 p.m.
10/12/2014



Configuración lista, click en Finish

ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd*]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

demo_1
xc6slx45-3csg484
demo_1 - Behavioral (demo_1.v

No Processes Running

Processes: demo_1 - Behavioral

Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope

```
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  entity main is
26      Port ( rst : in  STD_LOGIC;
27             clk : in  STD_LOGIC;
28             swt : in  STD_LOGIC_VECTOR (2 downto 0);
29             led : inout  STD_LOGIC_VECTOR (7 downto 0));
30  end main;
31
32  architecture Behavioral of main is
33
34     signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
35     signal dividedClk,clkout : STD_LOGIC;
36
37  begin
38
39     process (clk, rst) begin
40        if rst = '1' then clkdiv <= (others=>'0');
41           elsif clk = '1' and clk'Event then
42              clkdiv <= clkdiv + 1;
43              clkout <= dividedClk;
44           end if;
45     end process;
46
47     with swt select
48     dividedClk <= clkdiv(18) when "111",
49                   clkdiv(19) when "110",
50                   clkdiv(20) when "101",
```

Start Design Files Libraries

demo_1.vhd*

Design Summary

Console

```
Started : "Launching ISE Text Editor to edit demo_1.vhd".
Launching Design Summary/Report Viewer...
```

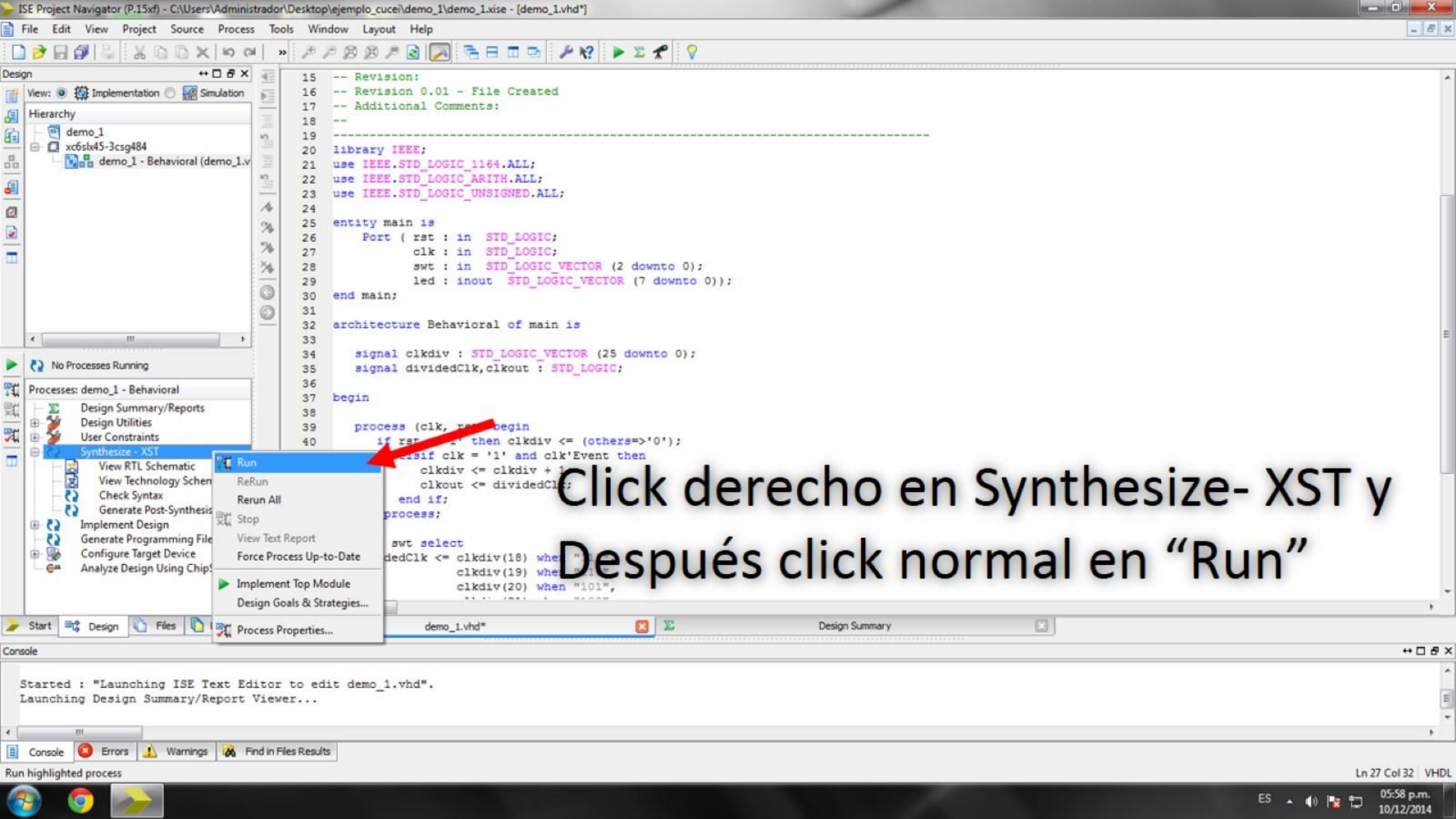
Hacer la programación en el archivo que nos abre

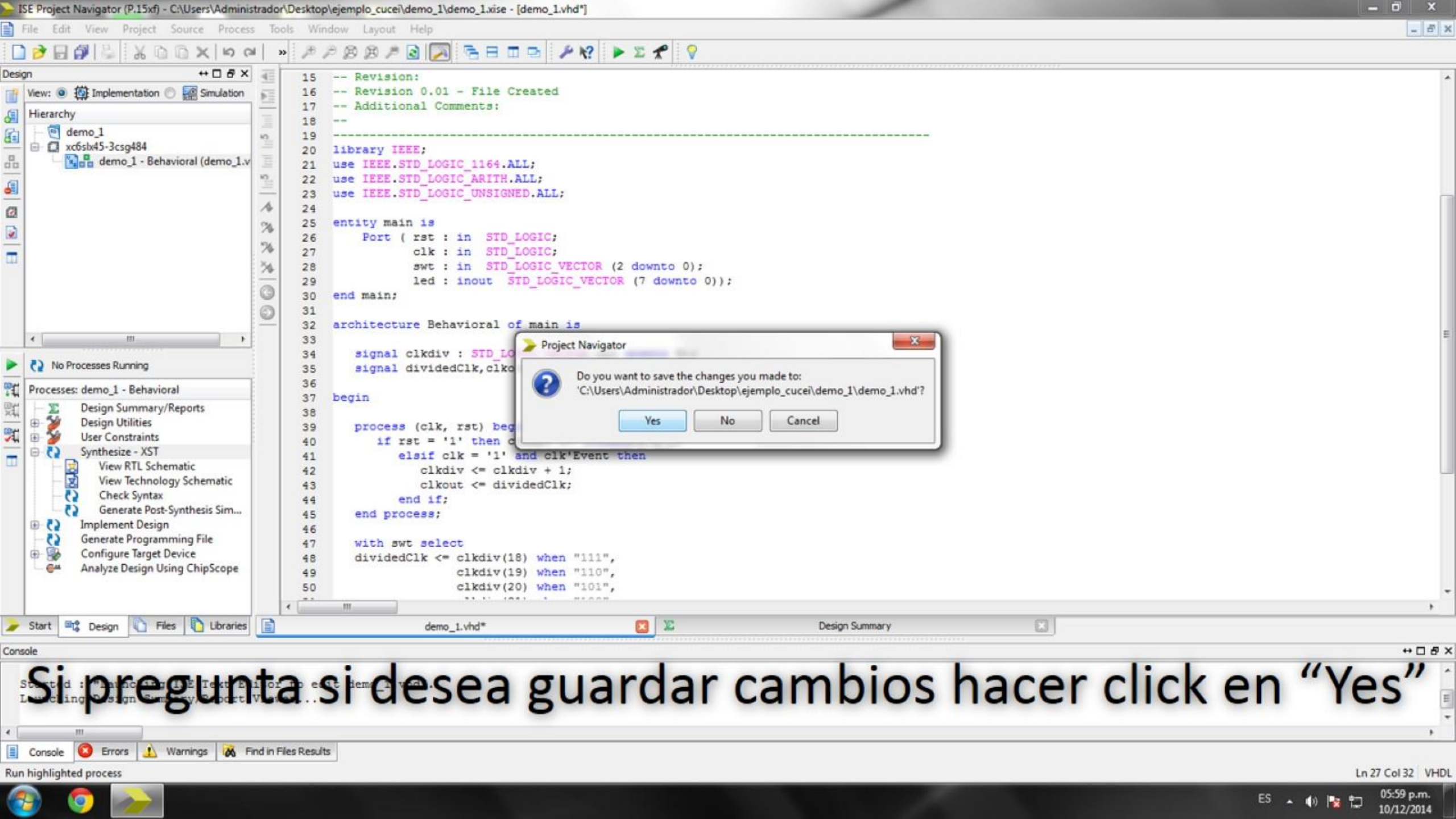
Console Errors Warnings Find in Files Results

Insert clipboard contents

Ln 27 Col 32 VHDL

ES 05:55 p.m. 10/12/2014


ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
demo_1 - Behavioral (demo_1.v
No Processes Running
Processes: demo_1 - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schen
Check Syntax
Generate Post-Synthesis
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using Chip
Run
ReRun
Rerun All
Stop
View Text Report
Force Process Up-to-Date
Implement Top Module
Design Goals & Strategies...
Process Properties...
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity main is
Port (rst : in STD_LOGIC;
clk : in STD_LOGIC;
swt : in STD_LOGIC_VECTOR (2 downto 0);
led : inout STD_LOGIC_VECTOR (7 downto 0));
end main;
architecture Behavioral of main is
signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
signal dividedClk,clkout : STD_LOGIC;
begin
Click derecho en Synthesize- XST y
Después click normal en “Run”
Start Design Files
demo_1.vhd*
Design Summary
Console
Started : "Launching ISE Text Editor to edit demo_1.vhd".
Launching Design Summary/Report Viewer...
Console Errors Warnings Find in Files Results
Run highlighted process
Ln 27 Col 32 VHDL
ES
05:58 p.m.
10/12/2014



Si pregunta si desea guardar cambios hacer click en “Yes”

ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- demo_1
- xc6slx45-3csg484
- main - Behavioral (demo_1.vhd)

No Processes Running

Processes: main - Behavioral

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis Sim...
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

```
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  entity main is
26      Port ( rst : in  STD_LOGIC;
27             clk : in  STD_LOGIC;
28             swt : in  STD_LOGIC_VECTOR (2 downto 0);
29             led : inout  STD_LOGIC_VECTOR (7 downto 0));
30  end main;
31
32  architecture Behavioral of main is
33
34     signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
35     signal dividedClk,clkout : STD_LOGIC;
36
37  begin
38
39     process (clk, rst) begin
40        if rst = '1' then clkdiv <= (others=>'0');
41           elsif clk = '1' and clk'Event then
42              clkdiv <= clkdiv + 1;
43              clkout <= dividedClk;
44           end if;
45     end process;
46
47     with swt select
48     dividedClk <= clkdiv(18) when "111",
49                   clkdiv(19) when "110",
50                   clkdiv(20) when "101",
```

Start Design Files Libraries

demo_1.vhd

Design Summary (Synthesized)

Console

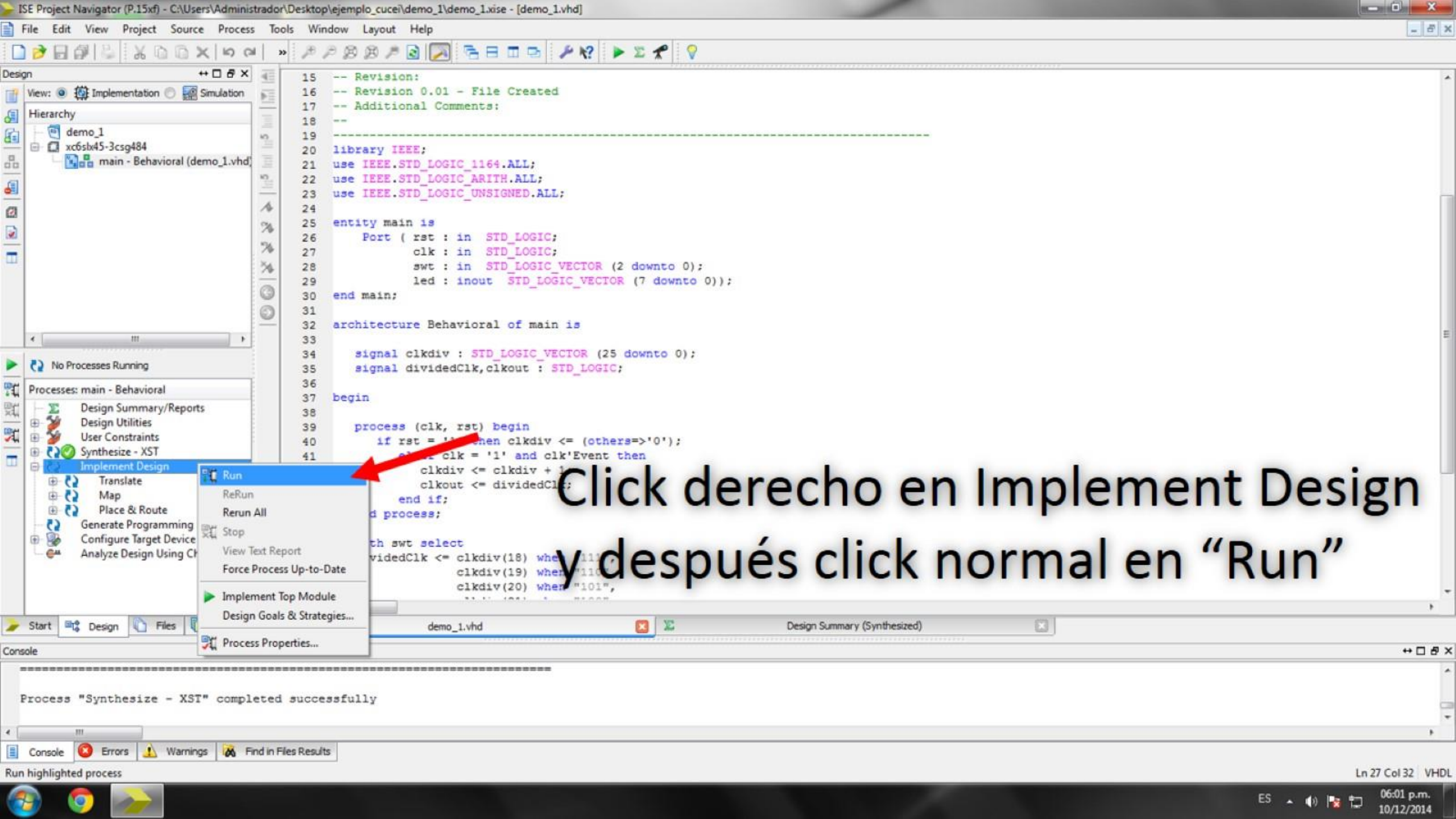
```
=========================================================================

Process "Synthesize - XST" completed successfully
```

Esperemos a que tenga palomita verde

Console Errors Warnings Find in Files Results

Ln 27 Col 32 VHDL

ES 06:00 p.m. 10/12/2014


ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
main - Behavioral (demo_1.vhd)
No Processes Running
Processes: main - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Translate
Map
Place & Route
Generate Programming
Configure Target Device
Analyze Design Using Ch
Run
ReRun
Rerun All
Stop
View Text Report
Force Process Up-to-Date
Implement Top Module
Design Goals & Strategies...
Process Properties...
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity main is
Port (rst : in STD_LOGIC;
clk : in STD_LOGIC;
swt : in STD_LOGIC_VECTOR (2 downto 0);
led : inout STD_LOGIC_VECTOR (7 downto 0));
end main;
architecture Behavioral of main is
signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
signal dividedClk,clkout : STD_LOGIC;
begin
Click derecho en Implement Design
y después click normal en “Run”
Start Design Files
demo_1.vhd
Design Summary (Synthesized)
Console
Process "Synthesize - XST" completed successfully
Console Errors Warnings Find in Files Results
Run highlighted process
Ln 27 Col 32 VHDL
ES
06:01 p.m.
10/12/2014

ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- demo_1
- xc6slx45-3csg484
- main - Behavioral (demo_1.vhd)

Running: Map

Processes: main - Behavioral

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design
  - Translate
  - Map
  - Place & Route
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

```
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  entity main is
26      Port ( rst : in  STD_LOGIC;
27             clk : in  STD_LOGIC;
28             swt : in  STD_LOGIC_VECTOR (2 downto 0);
29             led : inout  STD_LOGIC_VECTOR (7 downto 0));
30  end main;
31
32  architecture Behavioral of main is
33
34     signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
35     signal dividedClk,clkout : STD_LOGIC;
36
37  begin
38
39     process (clk, rst) begin
40        if rst = '1' then clkdiv <= (others=>'0');
41           elsif clk = '1' and clk'Event then
42              clkdiv <= clkdiv + 1;
43              clkout <= dividedClk;
44           end if;
45     end process;
46
47     with swt select
48     dividedClk <= clkdiv(18) when "111",
49                   clkdiv(19) when "110",
50                   clkdiv(20) when "101",
```

Esperamos....

(Puede tardar un poco)

Start Design Files Libraries

demo_1.vhd

Design Summary (running)

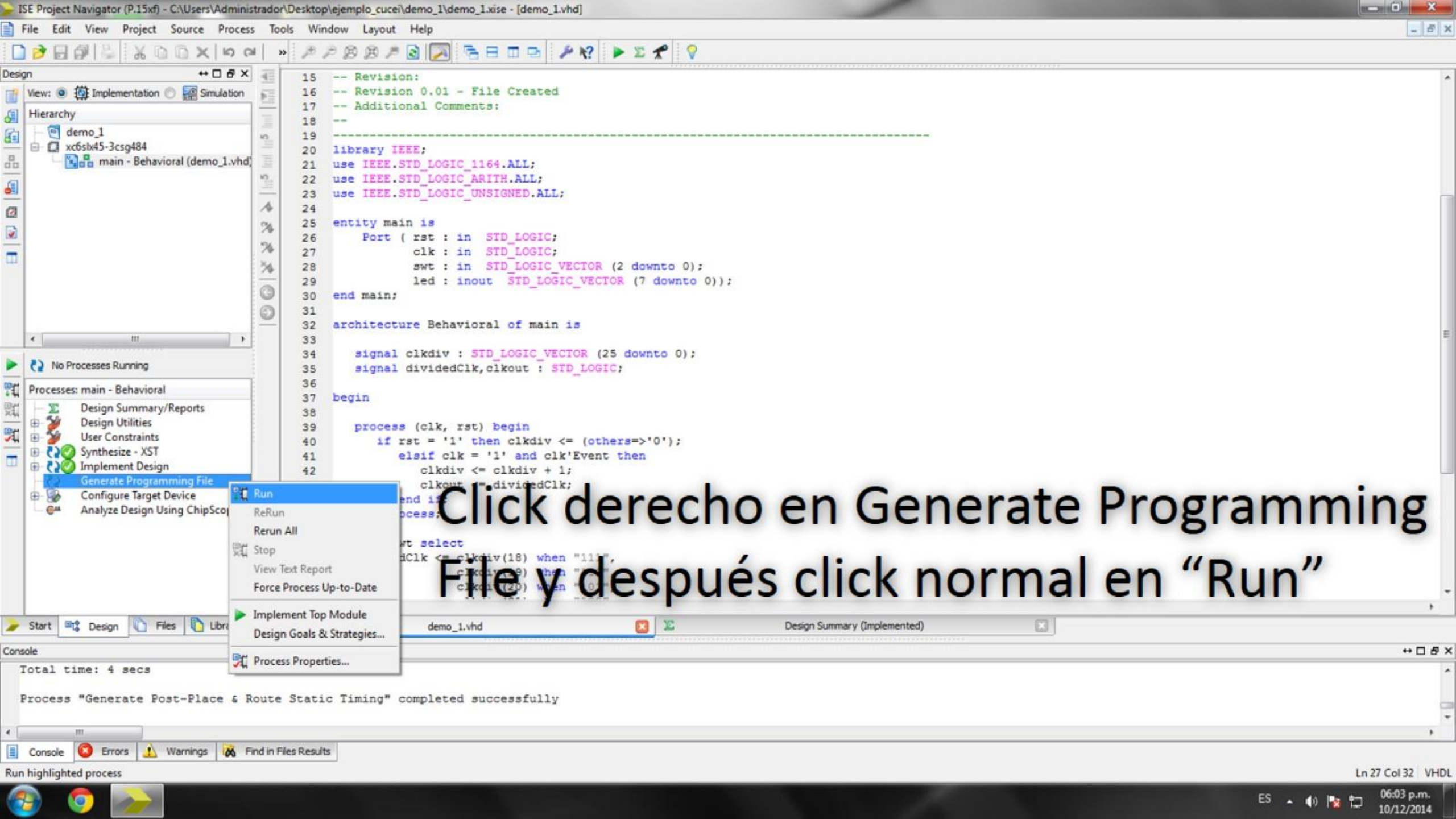
Console

```
Running map...
Command Line: map -intstyle ise -p xc6slx45-csg484-3 -w -logic_opt off -ol high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off -pr off -lc off -power off -o main_map.nc
Using target part "6slx45csg484-3".
```

Console Errors Warnings Find in Files Results

Ln 27 Col 32 VHDL

ES 06:02 p.m. 10/12/2014


ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
main - Behavioral (demo_1.vhd)
No Processes Running
Processes: main - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipSco
Run
ReRun
Rerun All
Stop
View Text Report
Force Process Up-to-Date
Implement Top Module
Design Goals & Strategies...
Process Properties...
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25 entity main is
26 Port (rst : in STD_LOGIC;
27 clk : in STD_LOGIC;
28 swt : in STD_LOGIC_VECTOR (2 downto 0);
29 led : inout STD_LOGIC_VECTOR (7 downto 0));
30 end main;
31
32 architecture Behavioral of main is
33
34 signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
35 signal dividedClk,clkout : STD_LOGIC;
36
37 begin
38
39 process (clk, rst) begin
40 if rst = '1' then clkdiv <= (others=>'0');
41 elsif clk = '1' and clk'Event then
42 clkdiv <= clkdiv + 1;
Click derecho en Generate Programming
File y después click normal en “Run”
Start Design Files
demo_1.vhd
Design Summary (Implemented)
Console
Total time: 4 secs
Process "Generate Post-Place & Route Static Timing" completed successfully
Console Errors Warnings Find in Files Results
Run highlighted process
Ln 27 Col 32 VHDL
ES
06:03 p.m.
10/12/2014

ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

demo_1
xc6slx45-3csg484
main - Behavioral (demo_1.vhd)

No Processes Running

Processes: main - Behavioral

Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope

```
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  entity main is
26      Port ( rst : in  STD_LOGIC;
27             clk : in  STD_LOGIC;
28             swt : in  STD_LOGIC_VECTOR (2 downto 0);
29             led : inout  STD_LOGIC_VECTOR (7 downto 0));
30  end main;
31
32  architecture Behavioral of main is
33
34     signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
35     signal dividedClk,clkout : STD_LOGIC;
36
37  begin
38
39     process (clk, rst) begin
40        if rst = '1' then clkdiv <= (others=>'0');
41           elsif clk = '1' and clk'Event then
42              clkdiv <= clkdiv + 1;
43              clkout <= dividedClk;
44           end if;
45     end process;
46
47     with swt select
48     dividedClk <= clkdiv(18) when "111",
49                   clkdiv(19) when "110",
50                   clkdiv(20) when "101",
```

Comprobamos que estén las 3 Palomitas verdes

Start Design Files Libraries

demo_1.vhd

Design Summary (Programming File Generated)

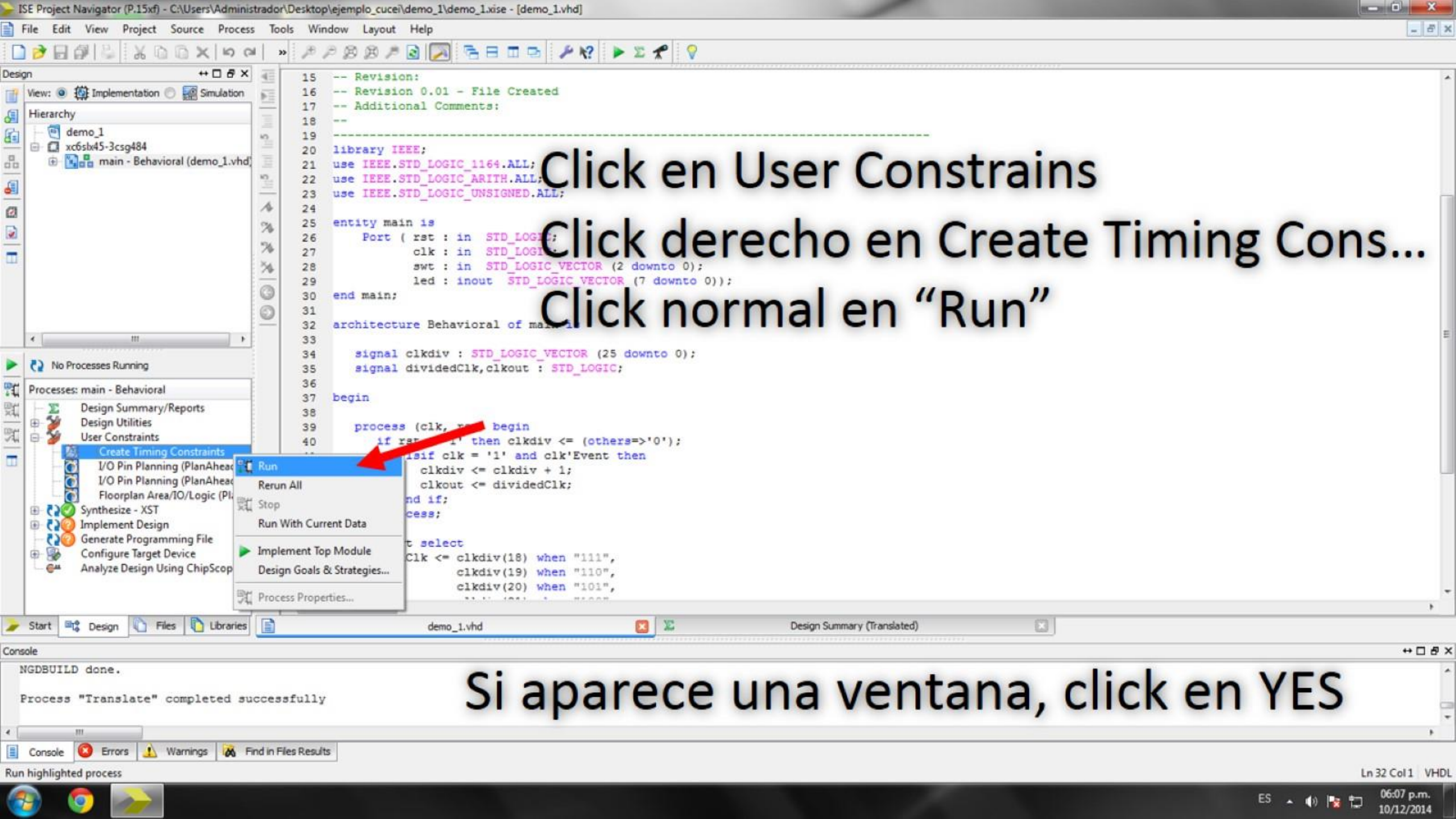
Console

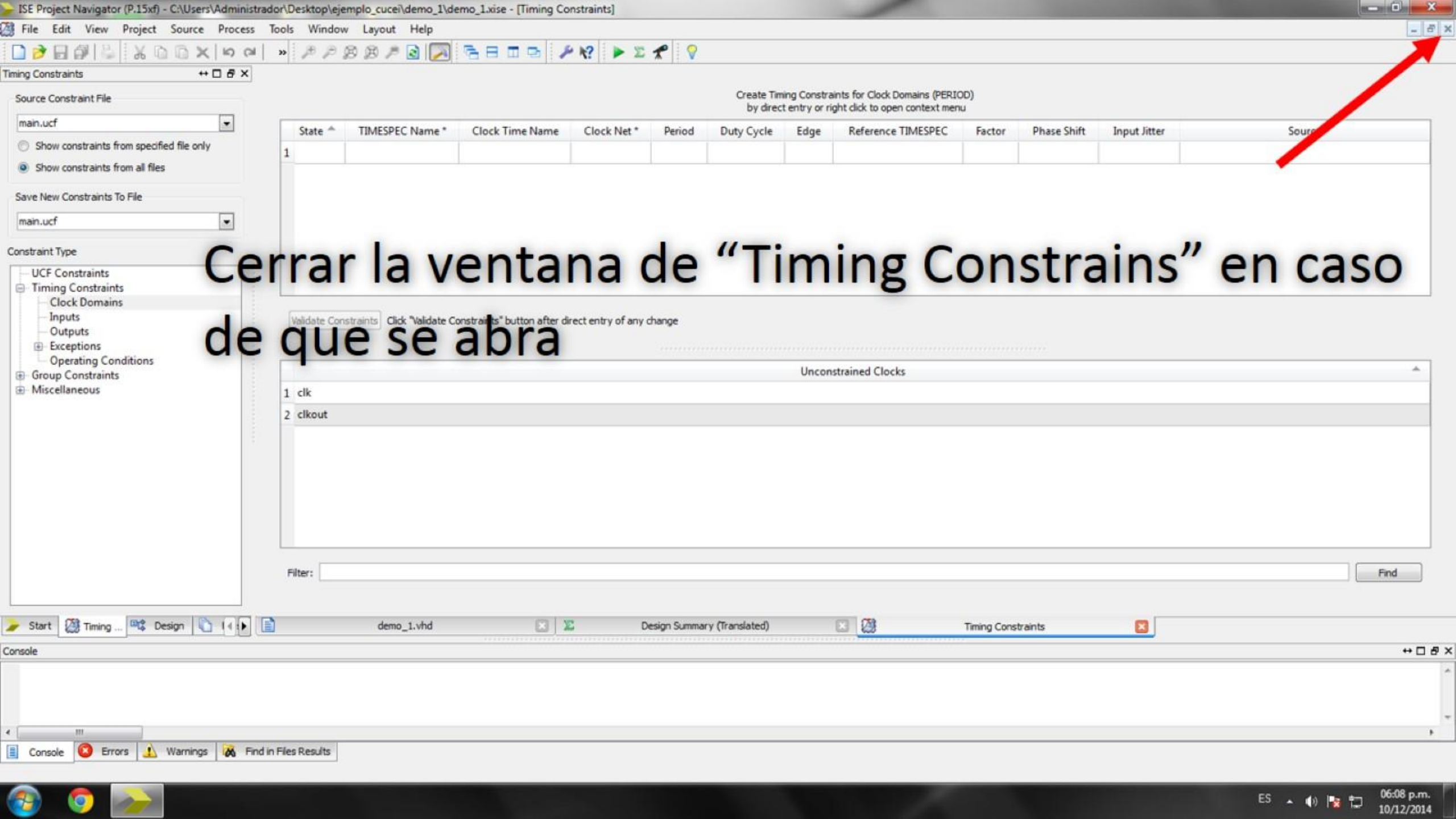
```
WebTalk is complete.

Process "Generate Programming File" completed successfully
```

Console Errors Warnings Find in Files Results

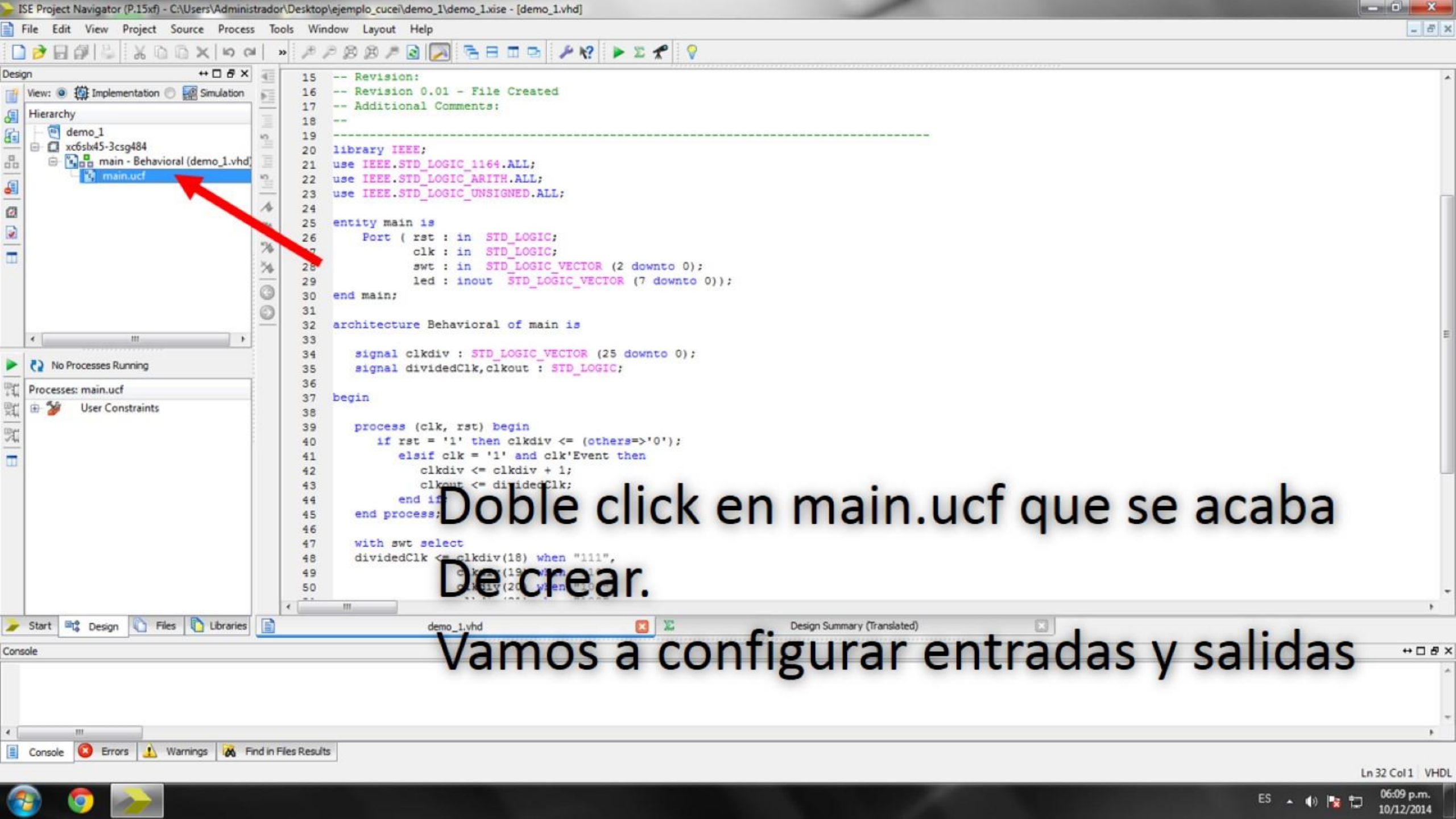
Ln 43 Col 1 VHDL

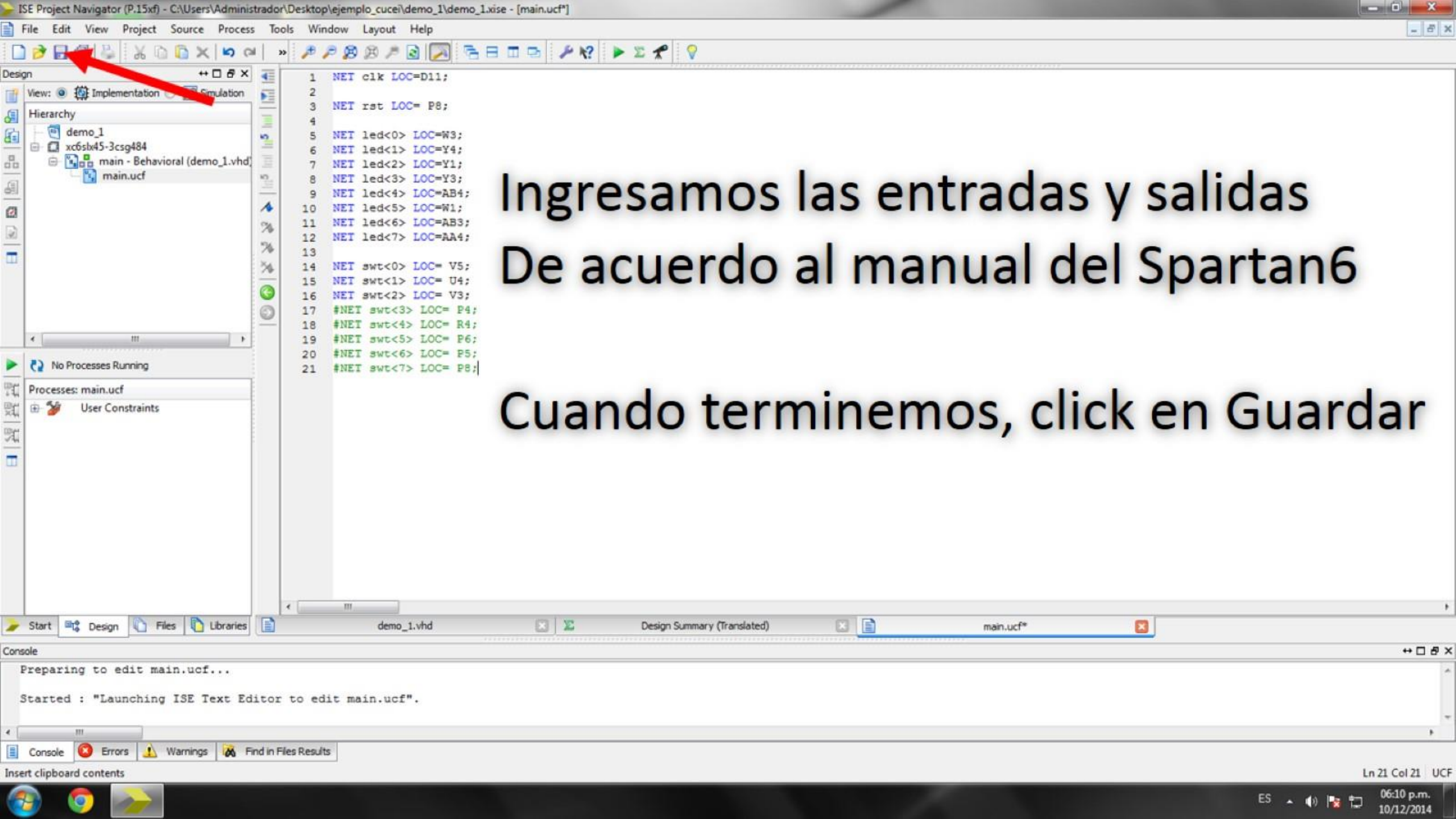
ES 06:04 p.m. 10/12/2014

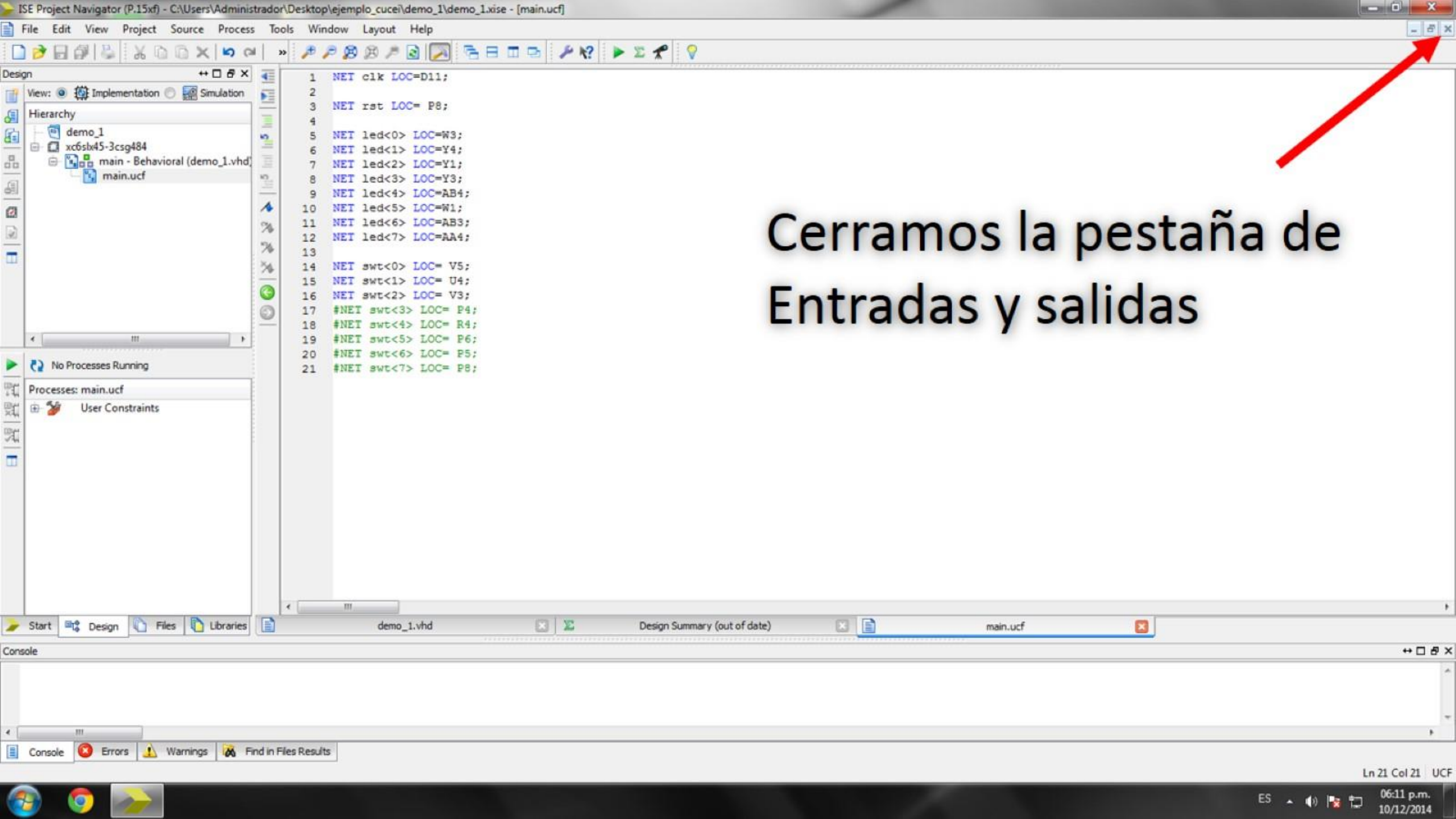

Click en User Constrains
Click derecho en Create Timing Cons...
Click normal en “Run”
Si aparece una ventana, click en YES
ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
main - Behavioral (demo_1.vhd)
No Processes Running
Processes: main - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Create Timing Constraints
I/O Pin Planning (PlanAhead)
I/O Pin Planning (PlanAhead)
Floorplan Area/IO/Logic (PlanAhead)
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Run
Rerun All
Stop
Run With Current Data
Implement Top Module
Design Goals & Strategies...
Process Properties...
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity main is
Port (rst : in STD_LOGIC;
clk : in STD_LOGIC;
swt : in STD_LOGIC_VECTOR (2 downto 0);
led : inout STD_LOGIC_VECTOR (7 downto 0));
end main;
architecture Behavioral of main is
signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
signal dividedClk,clkout : STD_LOGIC;
begin
process (clk,
if
elsif clk = '1' and clk'Event then
clkdiv <= clkdiv + 1;
clkout <= dividedClk;
end if;
process;
select
Clk <= clkdiv(18) when "111",
clkdiv(19) when "110",
clkdiv(20) when "101",
Start Design Files Libraries
demo_1.vhd
Design Summary (Translated)
Console
NGDBUILD done.
Process "Translate" completed successfully
Console Errors Warnings Find in Files Results
Run highlighted process
Ln 32 Col 1 VHDL
ES
06:07 p.m.
10/12/2014



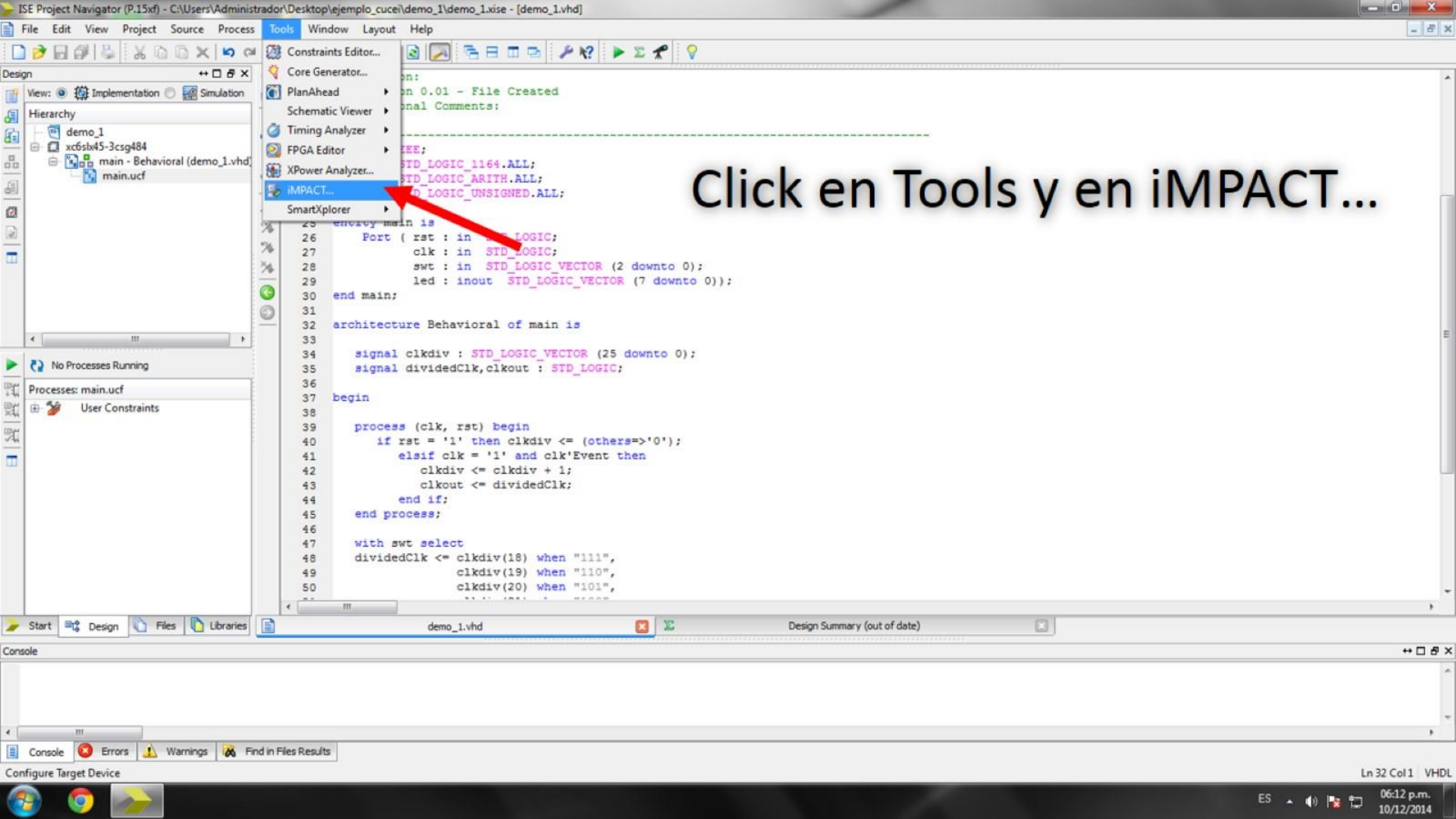
Cerrar la ventana de “Timing Constrains” en caso de que se abra

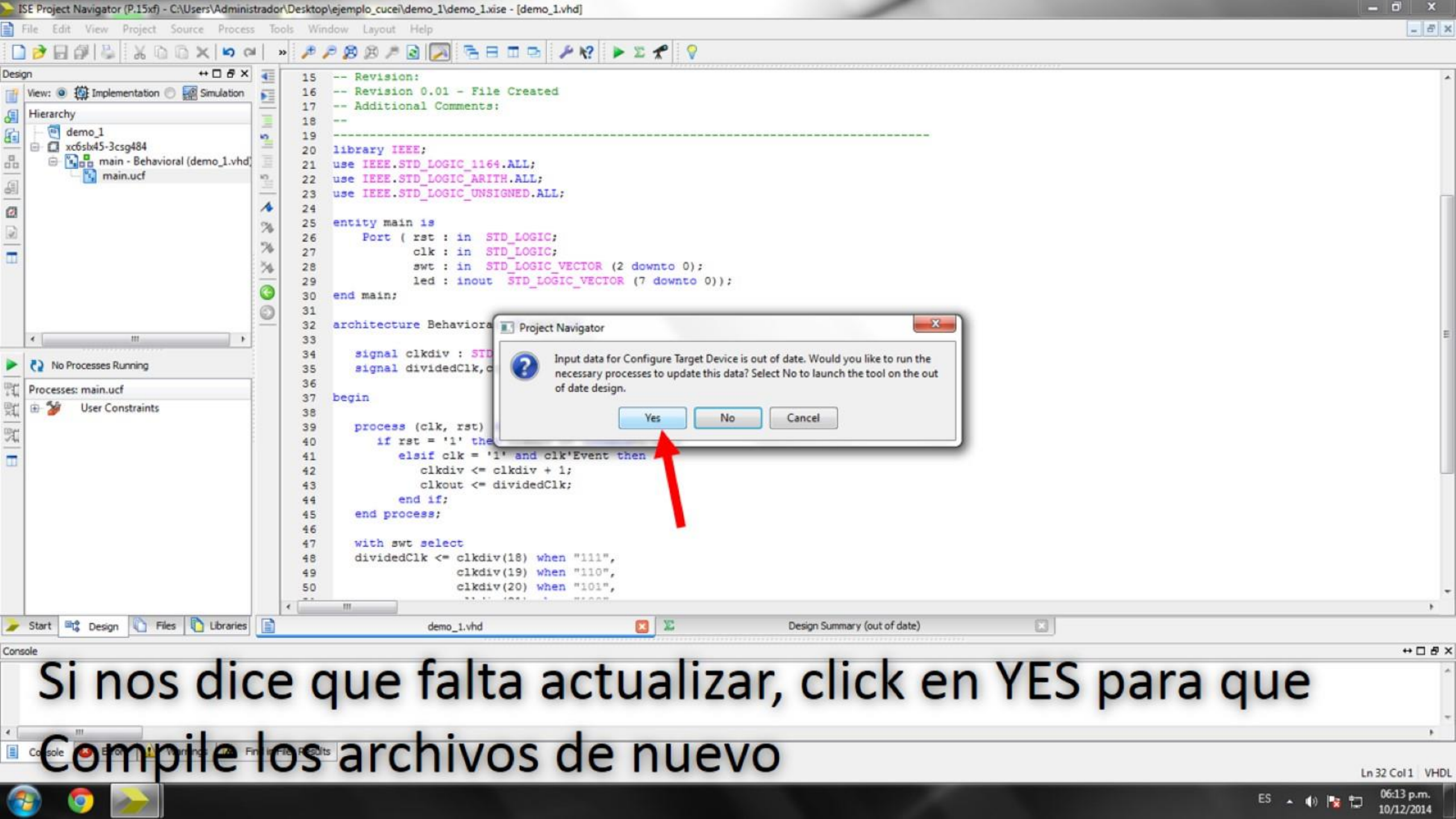

ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
main - Behavioral (demo_1.vhd)
main.ucf
No Processes Running
Processes: main.ucf
User Constraints
Start Design Files Libraries
demo_1.vhd
Design Summary (Translated)
Console
Console Errors Warnings Find in Files Results
Ln 32 Col 1 VHDL
Doble click en main.ucf que se acaba
De crear.
Vamos a configurar entradas y salidas


ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [main.ucf*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
main - Behavioral (demo_1.vhd)
main.ucf
No Processes Running
Processes: main.ucf
User Constraints
Start Design Files Libraries
1 NET clk LOC=D11;
2
3 NET rst LOC= P8;
4
5 NET led<0> LOC=W3;
6 NET led<1> LOC=Y4;
7 NET led<2> LOC=Y1;
8 NET led<3> LOC=Y3;
9 NET led<4> LOC=AB4;
10 NET led<5> LOC=W1;
11 NET led<6> LOC=AB3;
12 NET led<7> LOC=AA4;
13
14 NET swt<0> LOC= V5;
15 NET swt<1> LOC= U4;
16 NET swt<2> LOC= V3;
17 #NET swt<3> LOC= P4;
18 #NET swt<4> LOC= R4;
19 #NET swt<5> LOC= P6;
20 #NET swt<6> LOC= P5;
21 #NET swt<7> LOC= P8;
Ingresamos las entradas y salidas
De acuerdo al manual del Spartan6
Cuando terminemos, click en Guardar
demo_1.vhd
Design Summary (Translated)
main.ucf*
Console
Preparing to edit main.ucf...
Started : "Launching ISE Text Editor to edit main.ucf".
Console Errors Warnings Find in Files Results
Insert clipboard contents
Ln 21 Col 21 UCF
ES
06:10 p.m.
10/12/2014

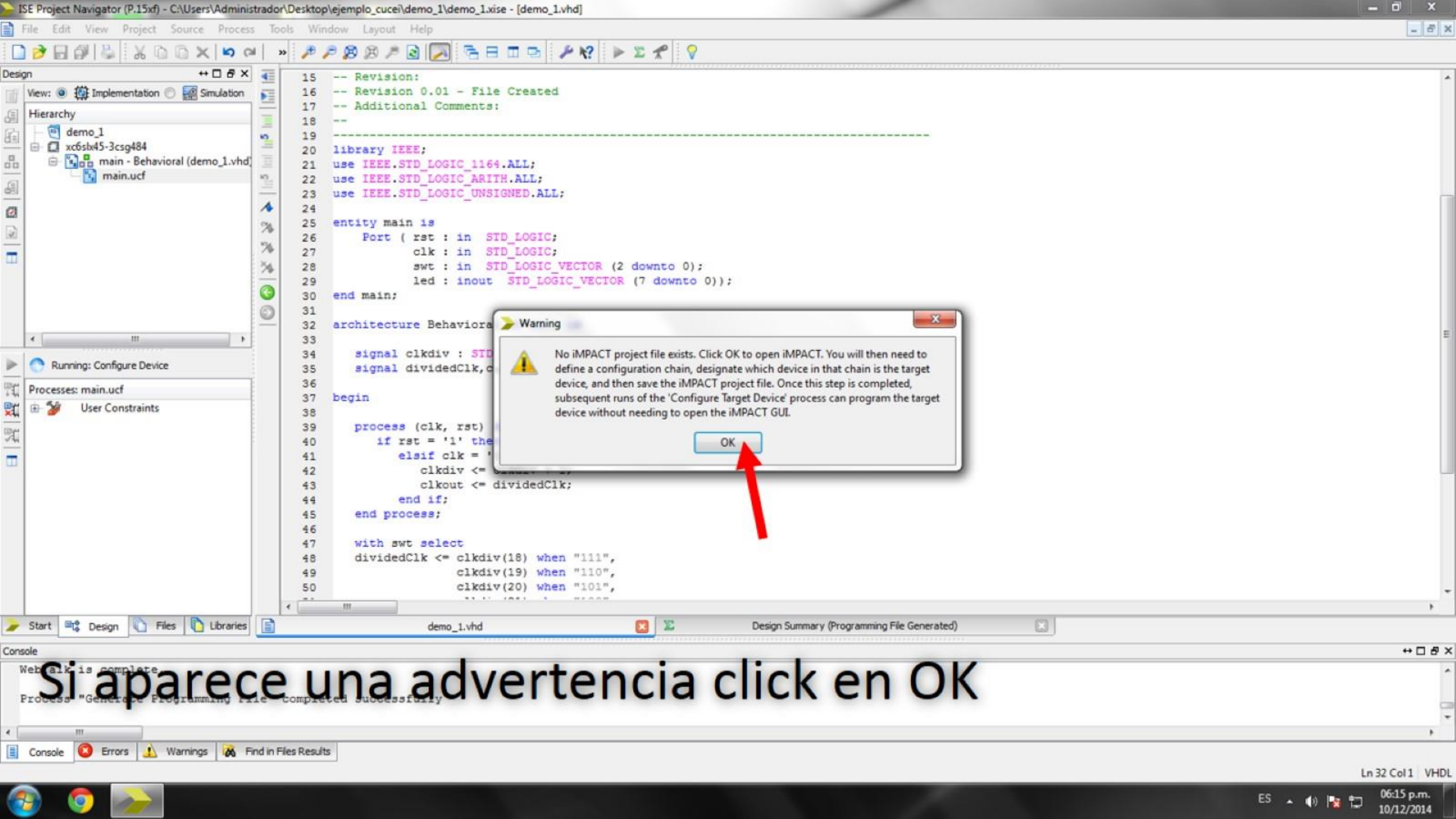


Cerramos la pestaña de Entradas y salidas

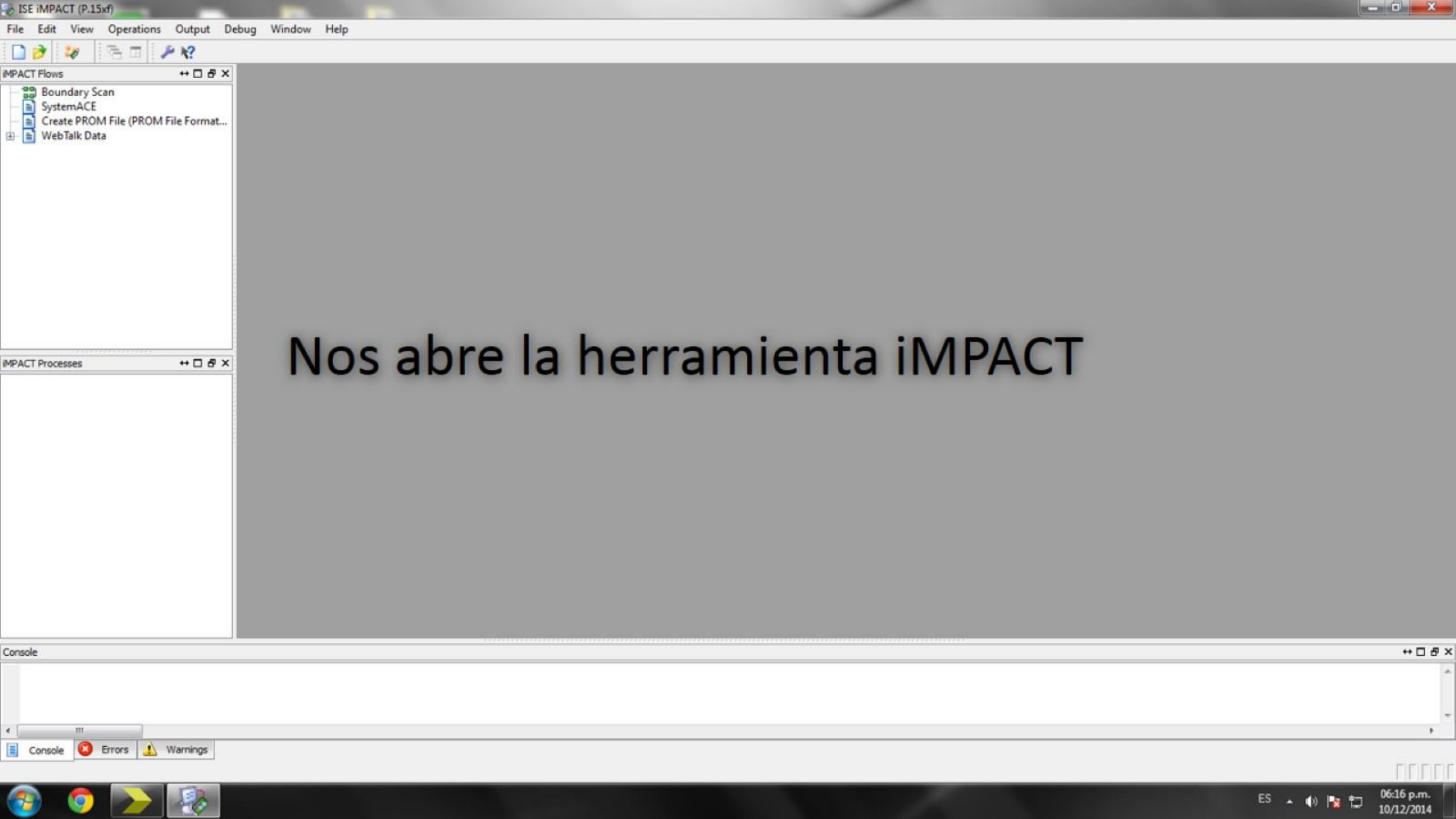

ISE Project Navigator (P.15xf) - C:\Users\Administrador\Desktop\ejemplo_cucei\demo_1\demo_1.xise - [demo_1.vhd]
File Edit View Project Source Process Tools Window Layout Help
Constraints Editor...
Core Generator...
PlanAhead
Schematic Viewer
Timing Analyzer
FPGA Editor
XPower Analyzer...
iMPACT...
SmartXplorer
Design
View: Implementation Simulation
Hierarchy
demo_1
xc6slx45-3csg484
main - Behavioral (demo_1.vhd)
main.ucf
No Processes Running
Processes: main.ucf
User Constraints
Click en Tools y en iMPACT...
entity main is
Port (rst : in STD_LOGIC;
clk : in STD_LOGIC;
swt : in STD_LOGIC_VECTOR (2 downto 0);
led : inout STD_LOGIC_VECTOR (7 downto 0));
end main;
architecture Behavioral of main is
signal clkdiv : STD_LOGIC_VECTOR (25 downto 0);
signal dividedClk,clkout : STD_LOGIC;
begin
process (clk, rst) begin
if rst = '1' then clkdiv <= (others=>'0');
elsif clk = '1' and clk'Event then
clkdiv <= clkdiv + 1;
clkout <= dividedClk;
end if;
end process;
with swt select
dividedClk <= clkdiv(18) when "111",
clkdiv(19) when "110",
clkdiv(20) when "101",
Start Design Files Libraries
demo_1.vhd
Design Summary (out of date)
Console
Console Errors Warnings Find in Files Results
Configure Target Device
Ln 32 Col 1 VHDL
ES
06:12 p.m.
10/12/2014

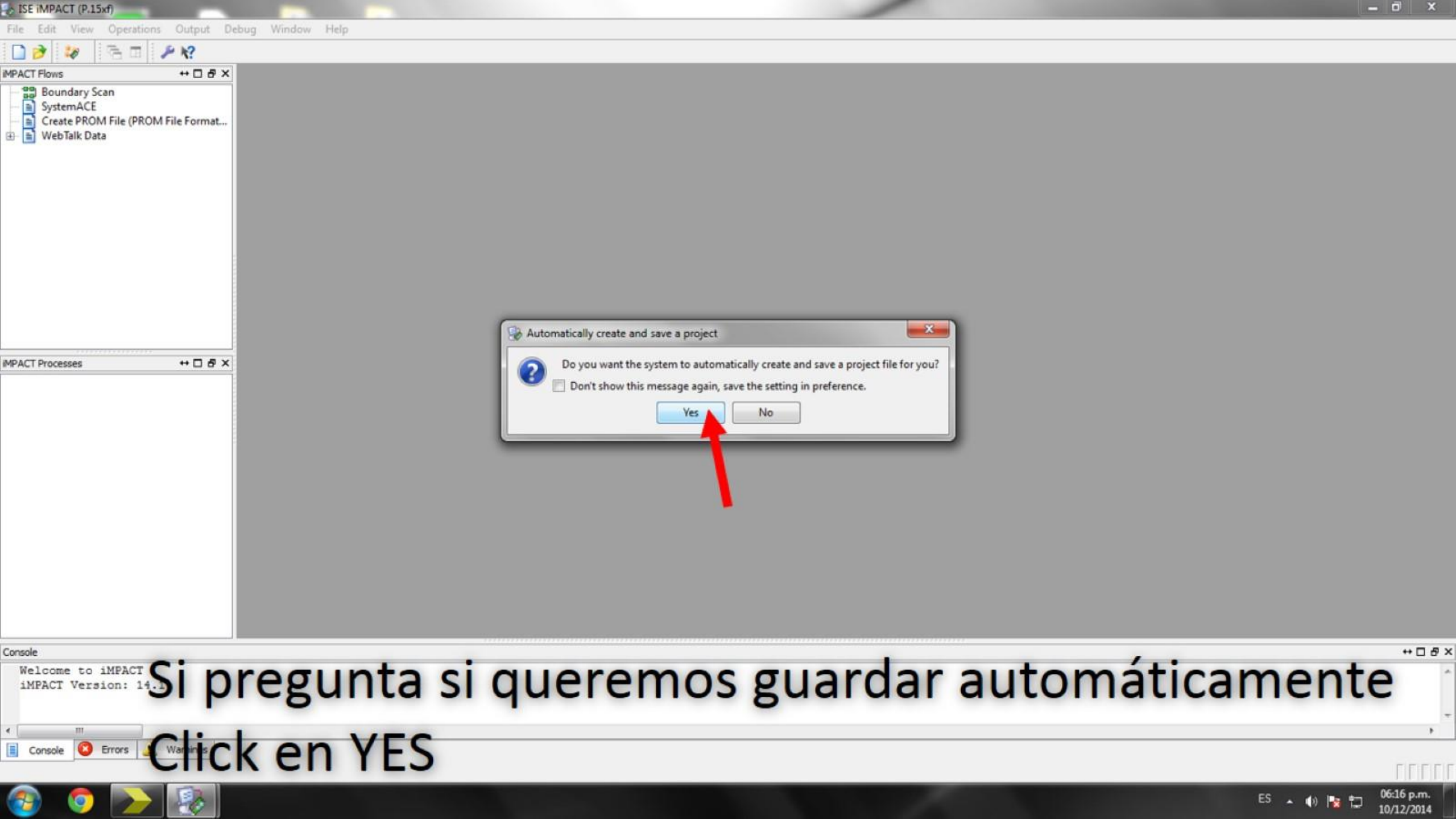


Si nos dice que falta actualizar, click en YES para que Compile los archivos de nuevo



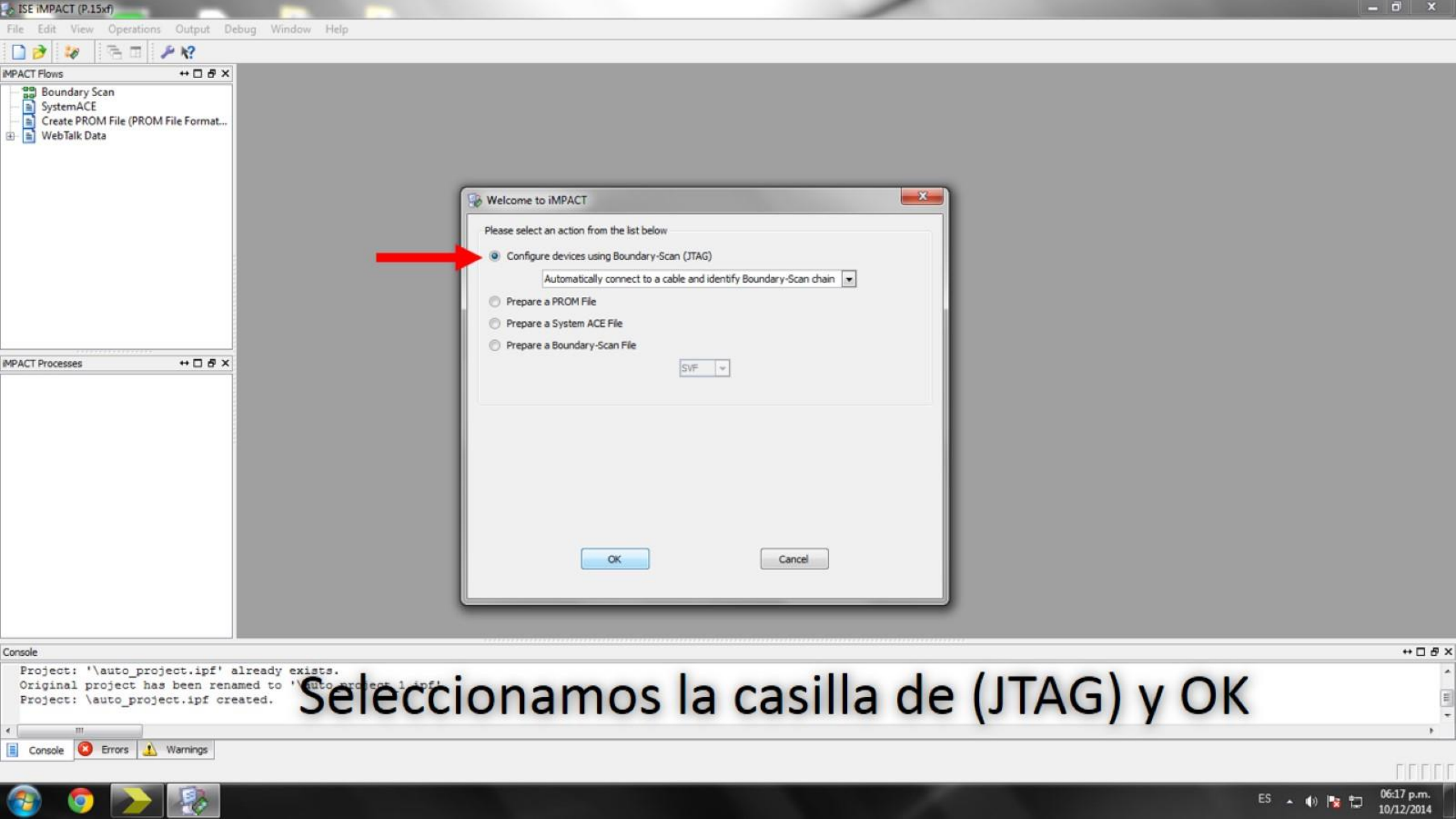
Si aparece una advertencia click en OK


ISE iMPACT (P.15xf)
File Edit View Operations Output Debug Window Help
iMPACT Flows
Boundary Scan
SystemACE
Create PROM File (PROM File Format...
WebTalk Data
iMPACT Processes
Nos abre la herramienta iMPACT
Console
Console Errors Warnings
ES
06:16 p.m.
10/12/2014



Si pregunta si queremos guardar automáticamente

Click en YES


ISE iMPACT (P.15xf)
File Edit View Operations Output Debug Window Help
iMPACT Flows
Boundary Scan
SystemACE
Create PROM File (PROM File Format...
WebTalk Data
iMPACT Processes
Welcome to iMPACT
Please select an action from the list below
Configure devices using Boundary-Scan (JTAG)
Automatically connect to a cable and identify Boundary-Scan chain
Prepare a PROM File
Prepare a System ACE File
Prepare a Boundary-Scan File
SVF
OK
Cancel
Console
Project: '\auto_project.ipf' already exists.
Original project has been renamed to '\auto_project_1.ipf'.
Project: \auto_project.ipf created.
Console
Errors
Warnings
Seleccionamos la casilla de (JTAG) y OK
ES
06:17 p.m.
10/12/2014

ISE iMPACT (P.15xf) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

iMPACT Flows

- Boundary Scan
- SystemACE
- Create PROM File (PROM File Format...
- WebTalk Data

iMPACT Processes

Available Operations are:

Right click device to select operations

TDI

xc6slx45
bypass

TDO

Auto Assign Configuration Files Query Dialog

Do you want to continue and assign configuration files(s)?

Don't show this message again, save the setting in preference.

Yes No

Identify Succeeded

Boundary Scan

Console

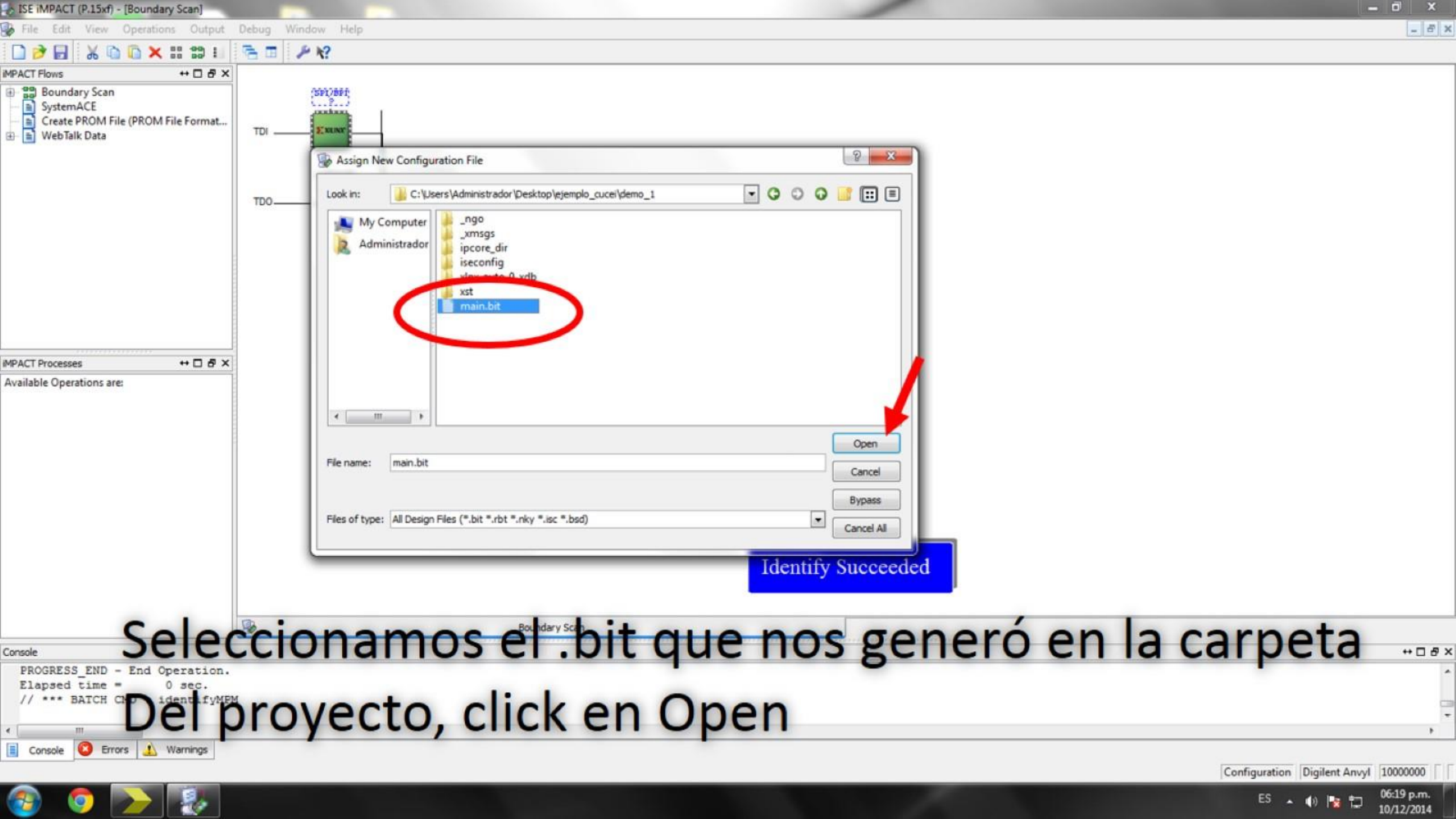
```
PROGRESS_END - End Operation.
Elapsed time =      0 sec.
// *** BATCH CMD : identifyMPM
```

Si pregunta si deseamos asignar, click en YES

Console Errors Warnings

Configuration Digilent Anvyl 10000000

ES 06:18 p.m. 10/12/2014



Seleccionamos el .bit que nos generó en la carpeta Del proyecto, click en Open

ISE iMPACT (P.15xf) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

iMPACT Flows

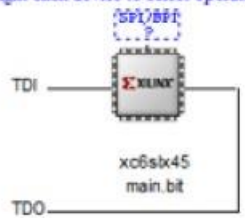
- Boundary Scan
- SystemACE
- Create PROM File (PROM File Format...
- WebTalk Data

iMPACT Processes

Available Operations are:

- Get Device ID
- Get Device Signature/Usercode
- Read Device Status
- Read Device DNA

Right click device to select operations



Identify Succeeded

Boundary Scan

Console

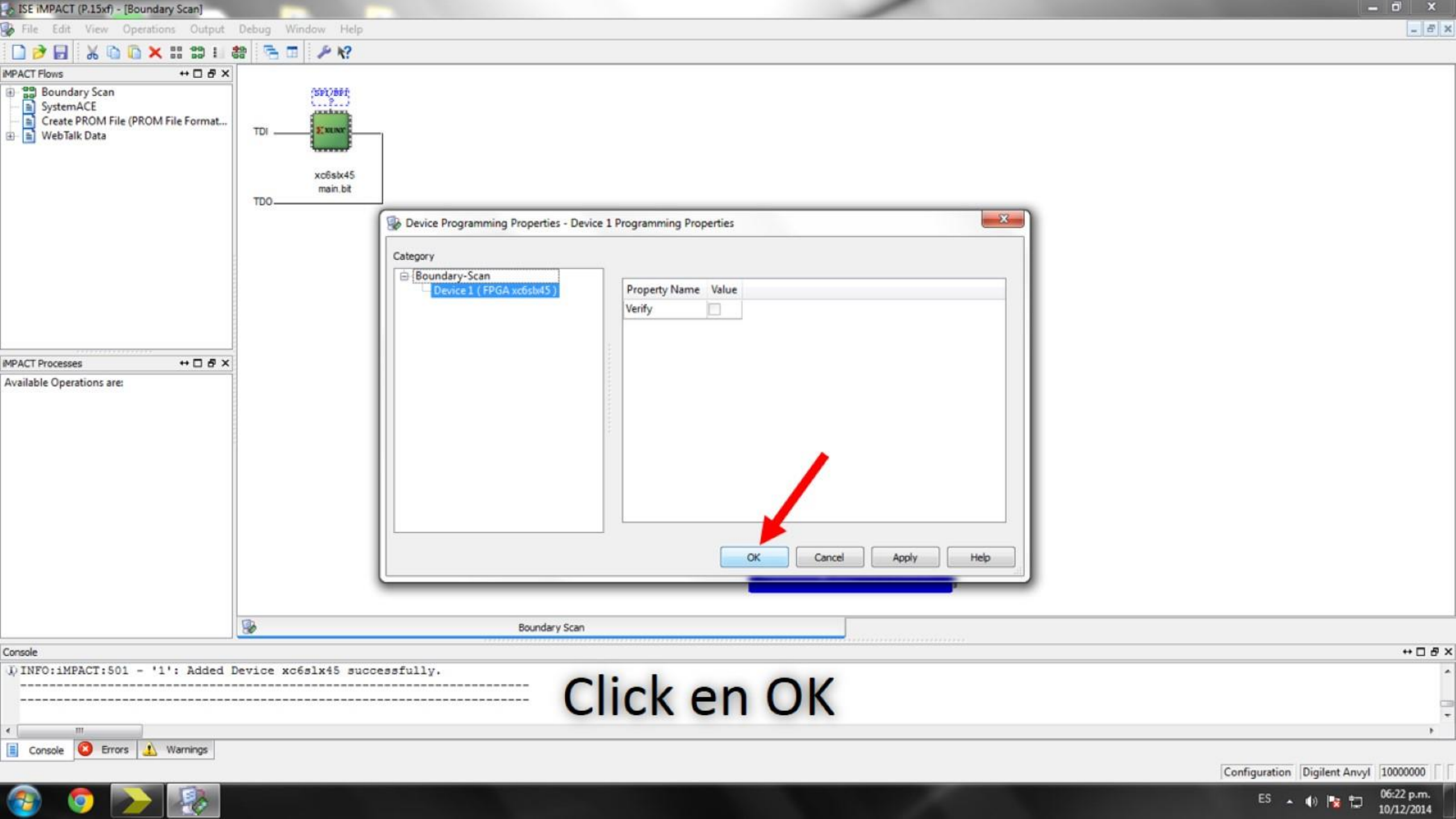
INFO:iMPACT:501 - '1': Added Device xc6slx45 successfully.

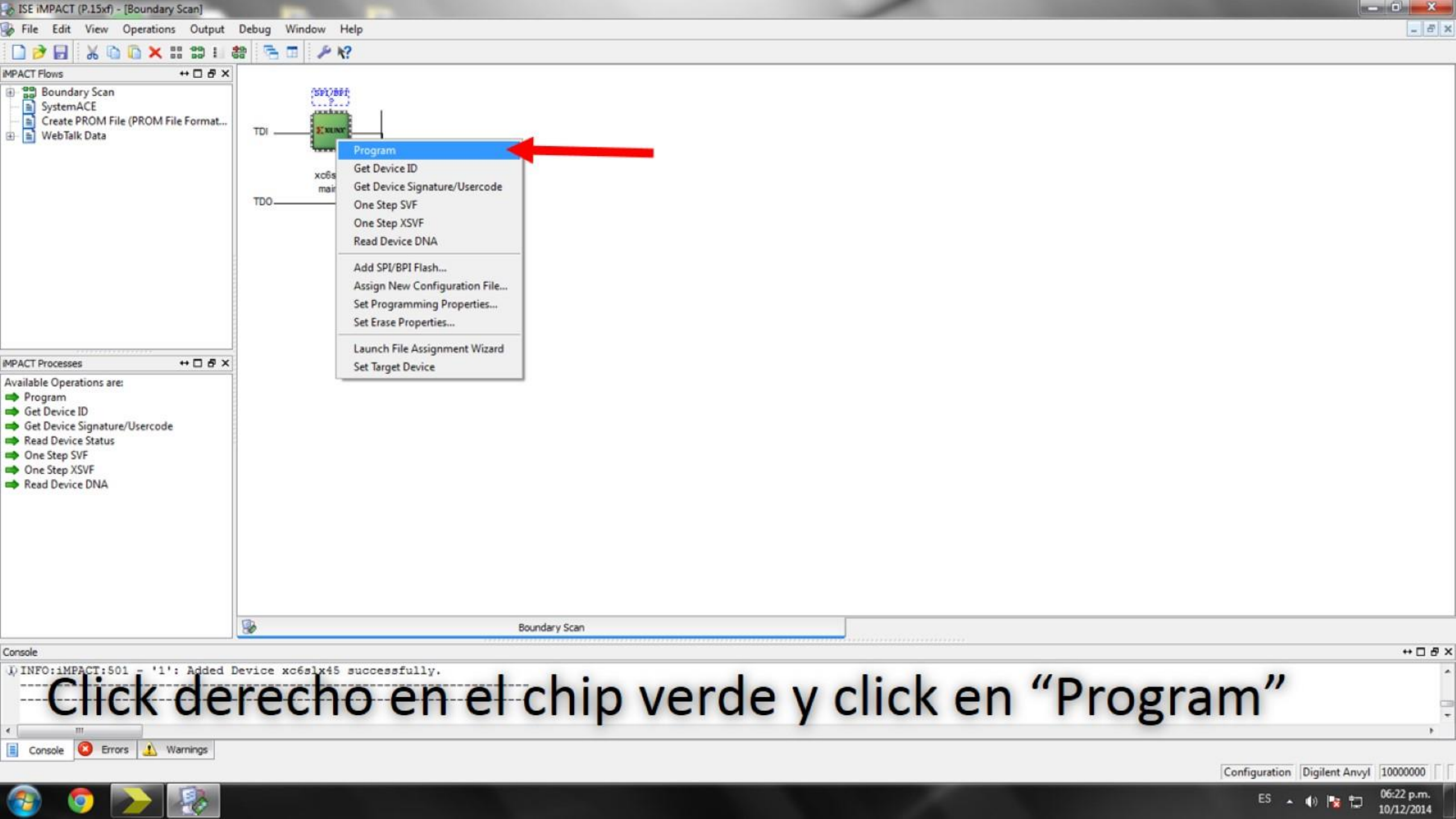
Si pregunta si queremos ligar a la memoria, click en NO

Console Errors Warnings

Configuration Digilent Anvyl 10000000

ES 06:20 p.m. 10/12/2014


ISE iMPACT (P.15xf) - [Boundary Scan]
File Edit View Operations Output Debug Window Help
iMPACT Flows
Boundary Scan
SystemACE
Create PROM File (PROM File Format...
WebTalk Data
iMPACT Processes
Available Operations are:
TDI
xc6slx45
main.bit
TDO
Device Programming Properties - Device 1 Programming Properties
Category
Boundary-Scan
Device 1 (FPGA xc6slx45)
Property Name
Value
Verify
OK
Cancel
Apply
Help
Boundary Scan
Console
INFO:iMPACT:501 - '1': Added Device xc6slx45 successfully.
Click en OK
Console
Errors
Warnings
Configuration
Digilent Anvyl
10000000
ES
06:22 p.m.
10/12/2014



Click derecho en el chip verde y click en “Program”

ISE iMPACT (P.15xf) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

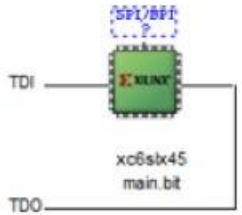
iMPACT Flows

- Boundary Scan
- SystemACE
- Create PROM File (PROM File Format...
- WebTalk Data

iMPACT Processes

Available Operations are:

- Program
- Get Device ID
- Get Device Signature/Usercode
- Read Device Status
- One Step SVF
- One Step XSVF
- Read Device DNA



Program Succeeded

Boundary Scan

Console

```
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =      1 sec.
```

"Programación Satisfactoria"

Console Errors Warnings

Configuration Digilent Anvyl 10000000

ES 06:23 p.m. 10/12/2014